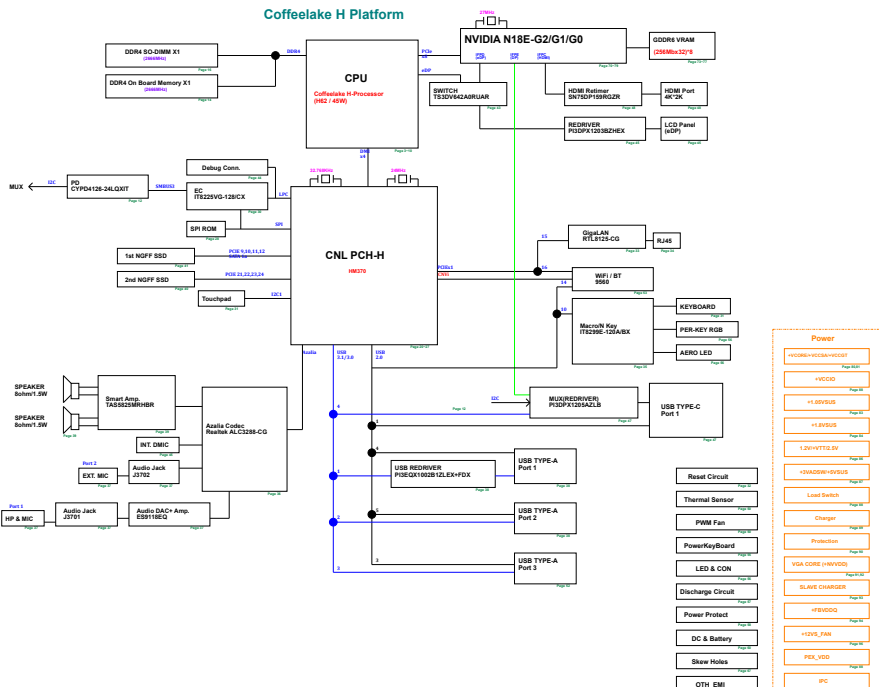


GX502/GU502 Block Diagram



dGPU
(AC-CAP Place on dGPU)

Trace length < 400 MILLS
Trace width = 12 MILLS
Trace spacing = 15 MILLS

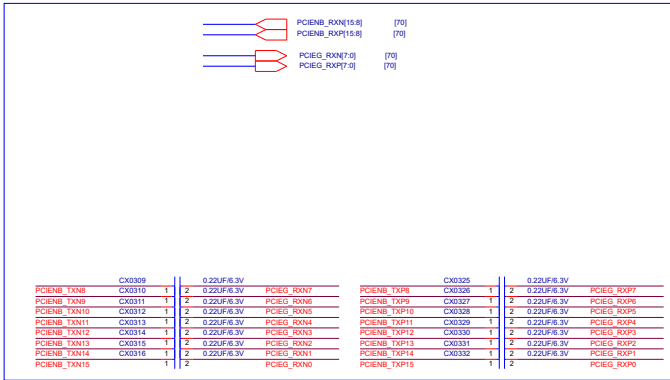
Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.For example:
 - When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

R0.1-25



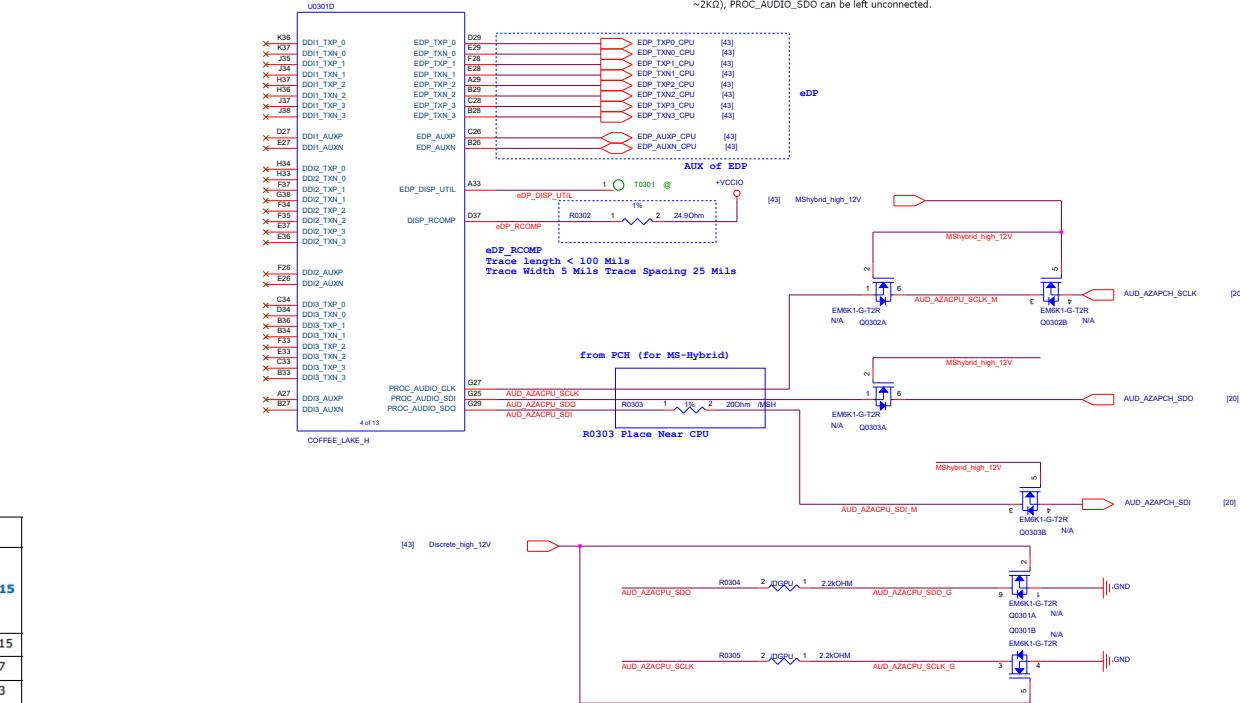
Display

2017/11/16 Add HDMI/TBT/eDP interface for MS-Hybrid by James

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ). PROC_AUDIO_SDO can be left unconnected.



31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ). PROC_AUDIO_SDO can be left unconnected.

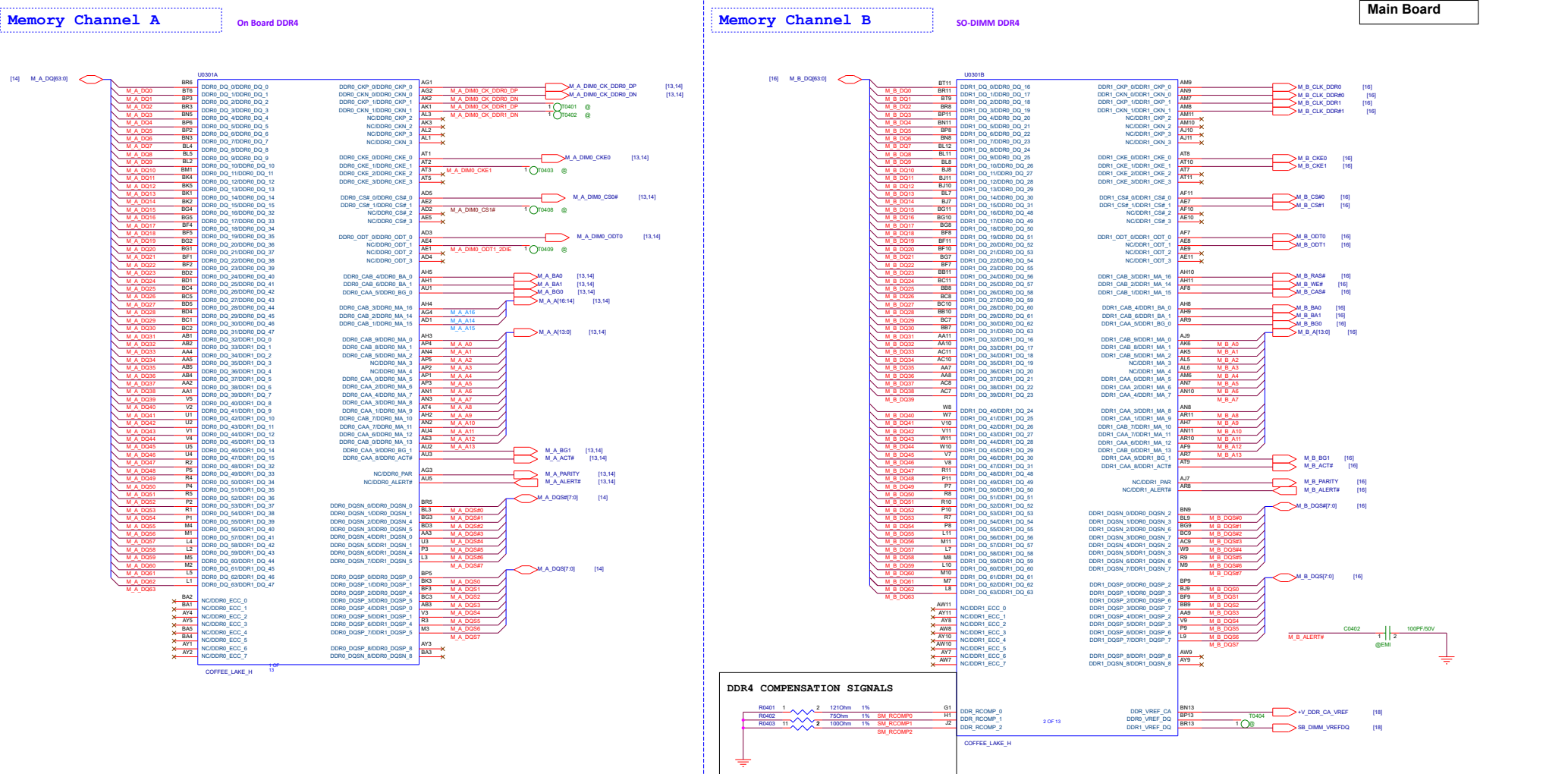
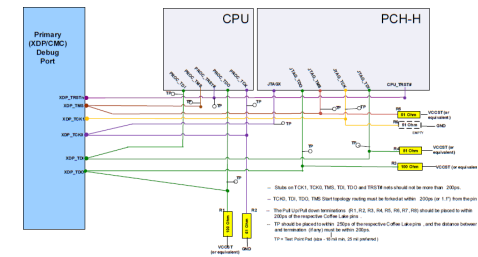
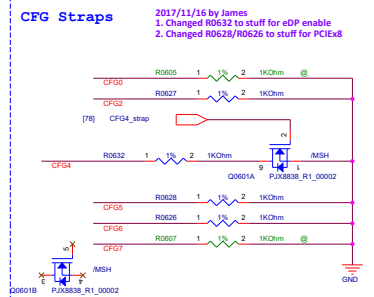
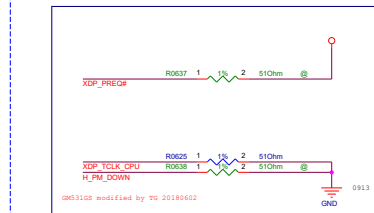
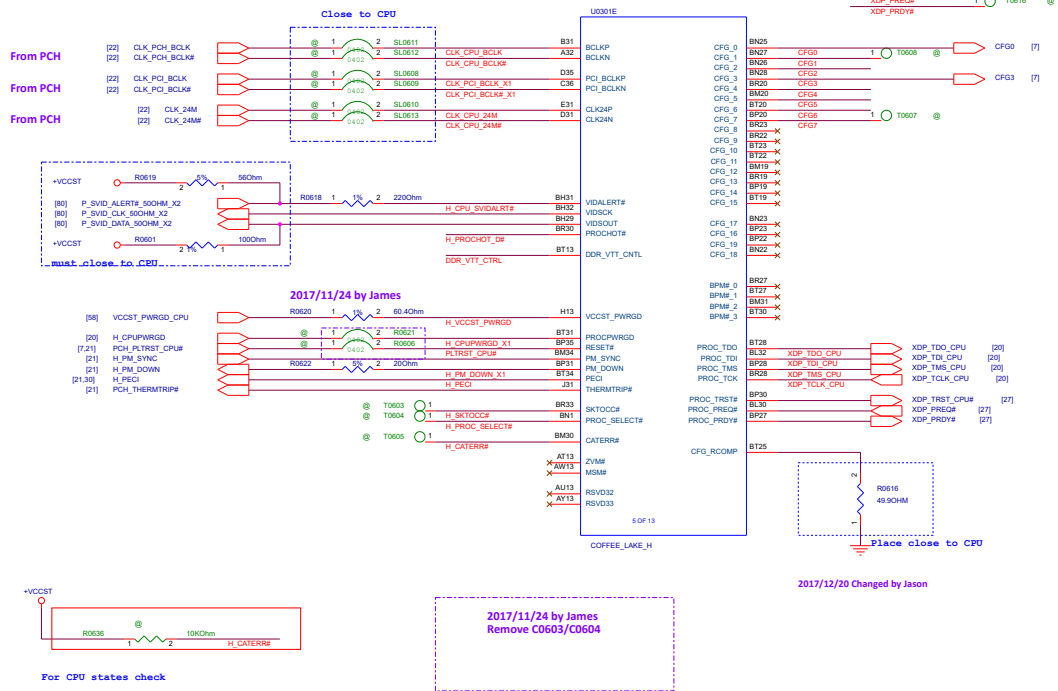


Figure 4-16. CFL-H DDR4 x8 Memory Down Placement and Block Diagram

www.teknisi-indonesia.com



Note: Connect JTAG pull-ups to Vcc5T on U/Y and S designs and Vcc5T-G on H designs.

CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express

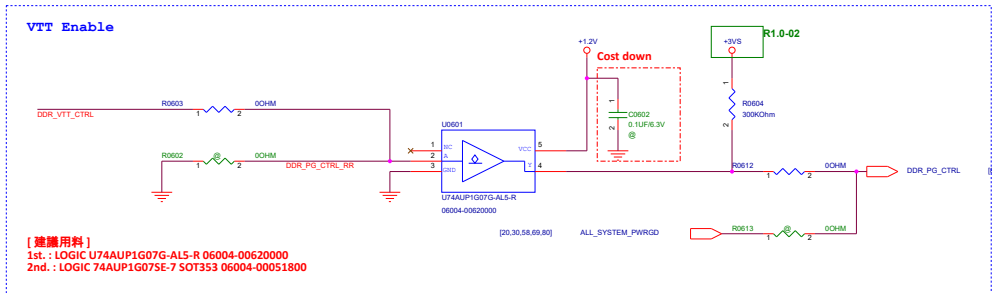
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

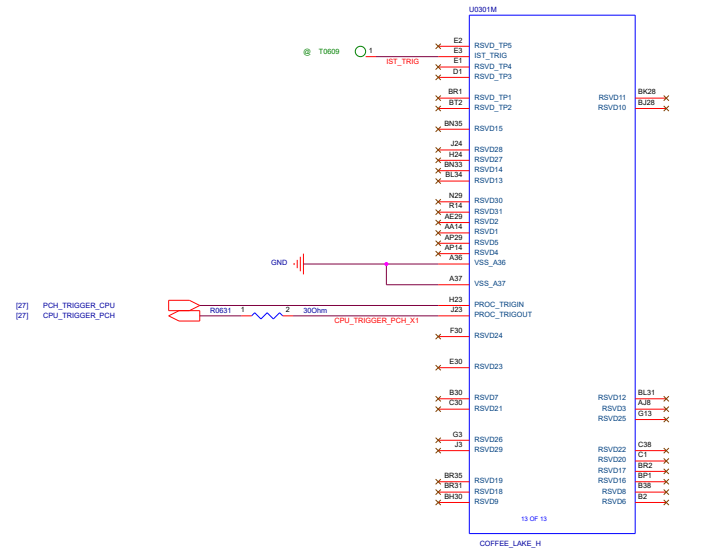
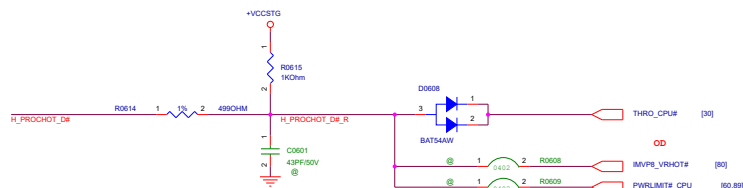
- 1 : (Default) PEG Train Imm

CFG[19:8] : Reserved Conf

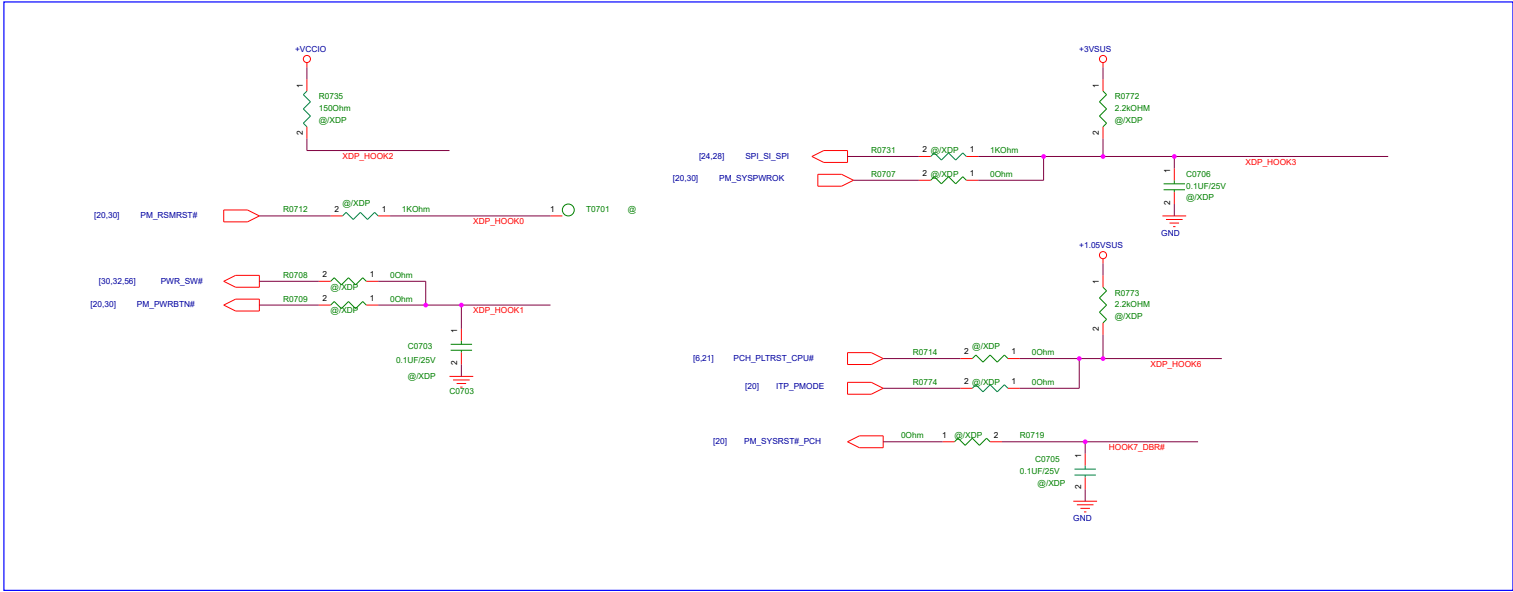
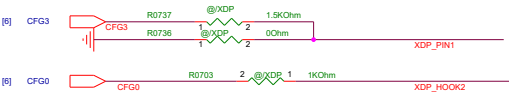
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

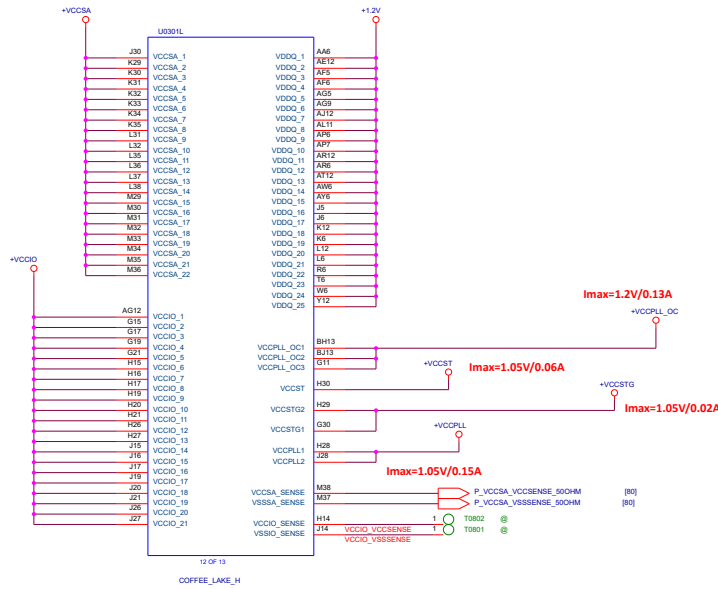


CPU SIDEBAND SIGNALS



CPU XDP



I_{max}=1.05V/11.1AI_{max}=1.2V/3.3A

Domain	Board Edge cap	Backside cap	Notes
VCCST		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route VCCST closest adjacent layer over any power net other than ground.
VCCSTG		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail.
VCCPLL		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
		1x 22uF/47uF 0805 (placeholder)	*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
VCCPLL_OC		2x 1uF 0201	Must be Ground referenced. Share with VDDQ. Board resistance from BGA to Power gate should be less than 86mOhm.

Domain	Board Edge cap	Backside cap	Notes
VCCSA	2x 47uF 0805 2x 22uF 0603		
VDDQ		7x 10uF 0402 1x 1uF 0201 4x 22uF 0603 11x 10uF 0402	
VCCIO		3x 10uF 0402	
VCCST		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
VCCSTG		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route VCCSTG closest adjacent layer over any power net other than ground.
VCCPLL		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
		1x 22uF/47uF 0805 (placeholder)	*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
VCCPLL_OC		2x 1uF 0201	Must be Ground referenced. Share with VDDQ. Board resistance from BGA to Power gate should be less than 86mOhm.

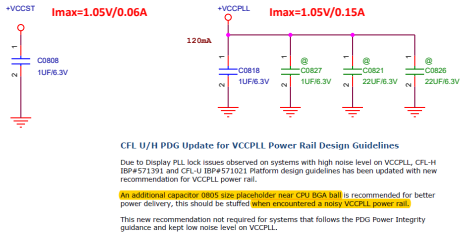
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0x	On in S0x	+3-10mW

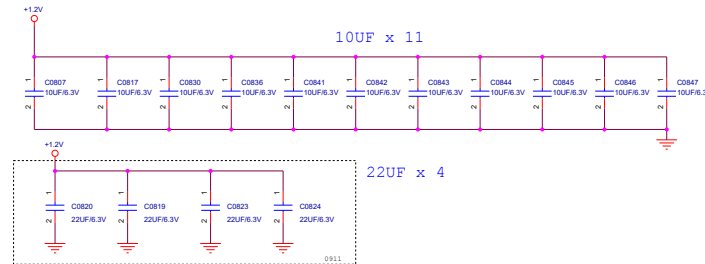
Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, Implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

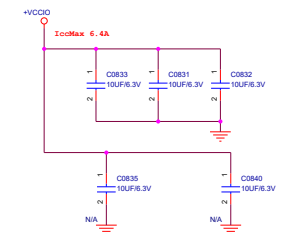
+VCCST/+VCCPLL DECAPS Place Back Side (TOP)



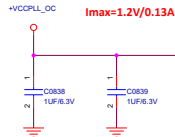
+VDDQ DECAPS Place Back Side (TOP)

I_{max}=1.2V/3.3A

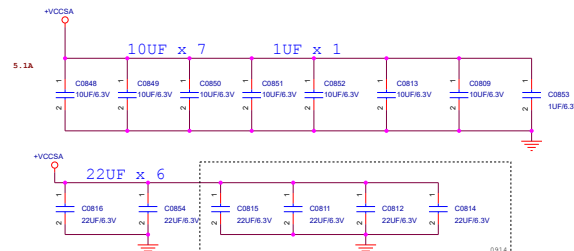
+VCCIO DECAPS Place Back Side (TOP)

I_{max}=0.95V/6.4A

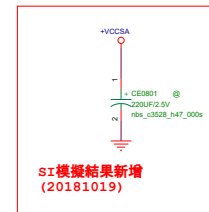
+VCCPLL_OC DECAPS Place Back Side (TOP)



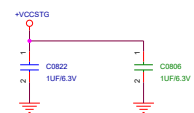
+VCCSA DECAPS Place Back Side (TOP)

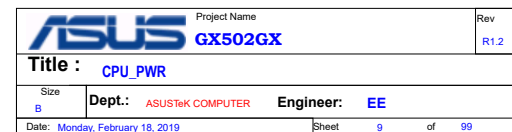
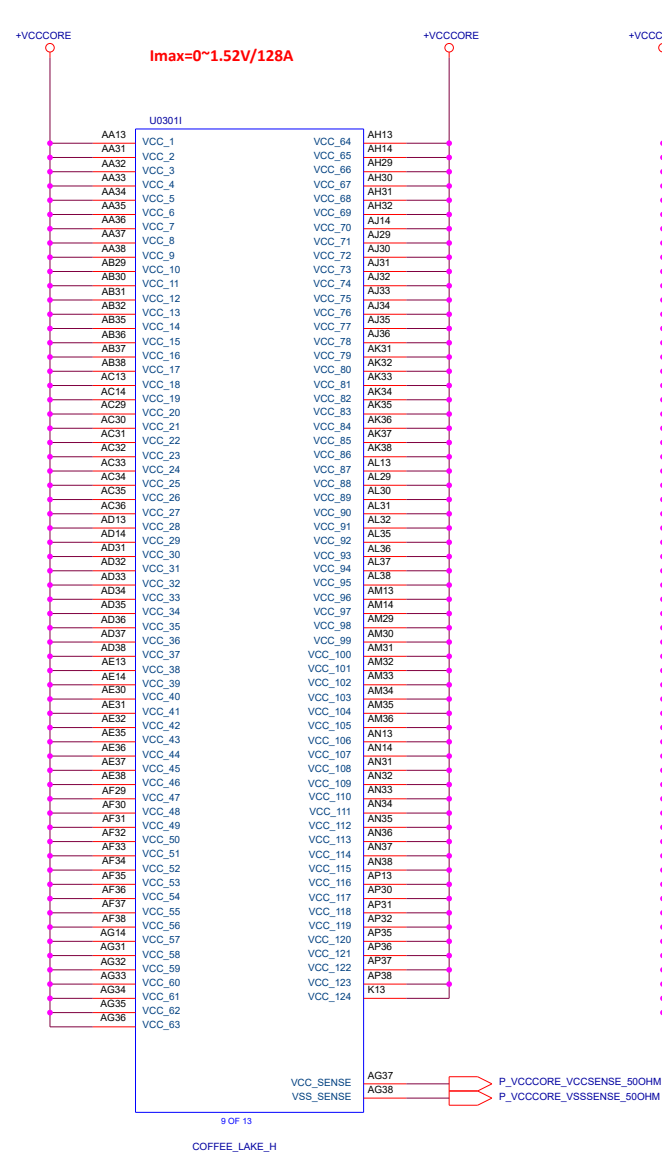
I_{max}=1.05V/11.1A

+VCCSA near CPU

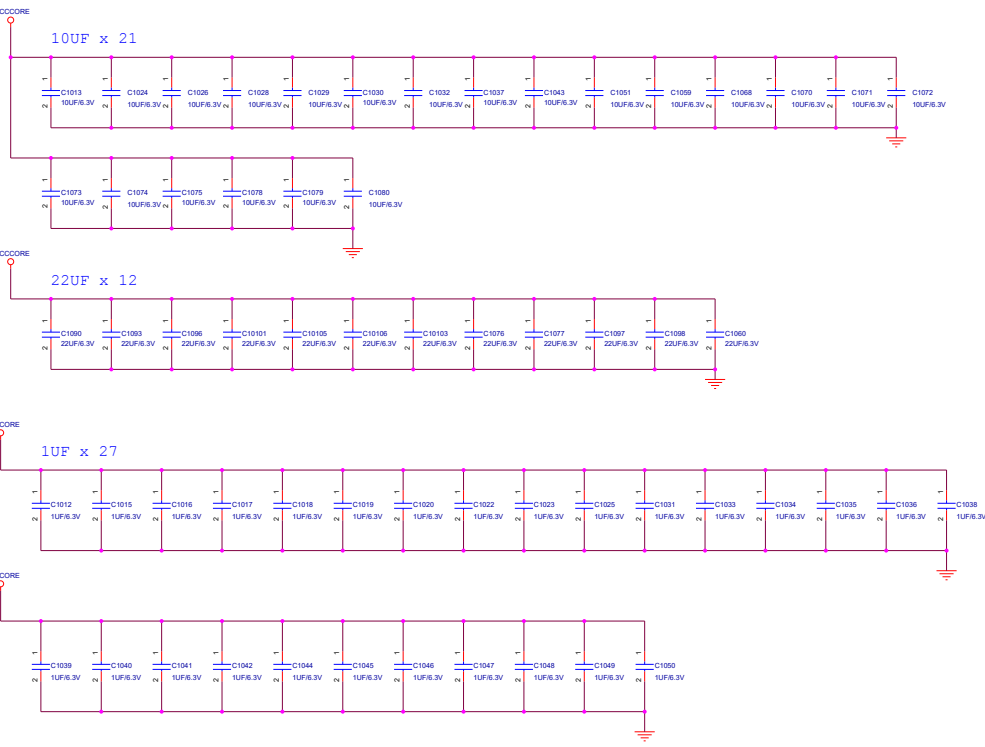


+VCCSTG DECAPS Place Back Side (TOP)

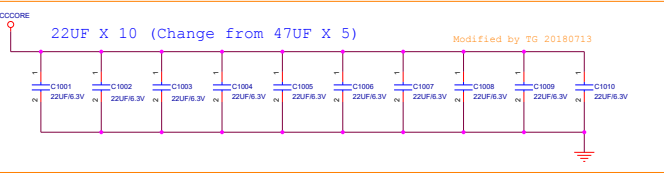




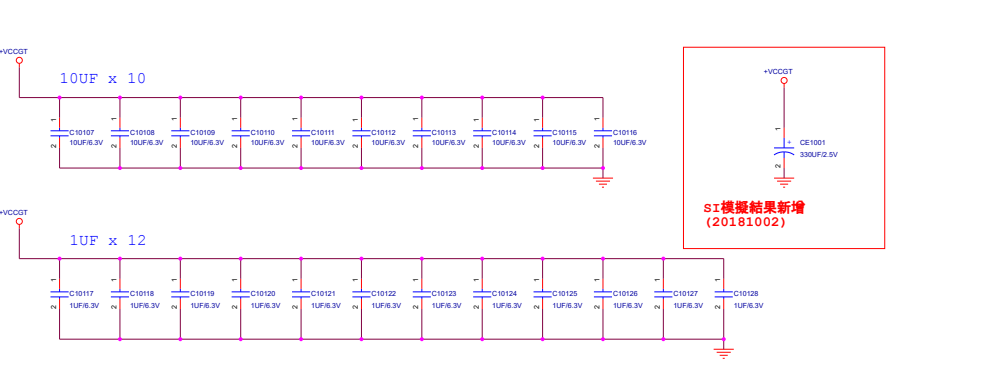
+VCCORE DECAPS Place Back Side (TOP)



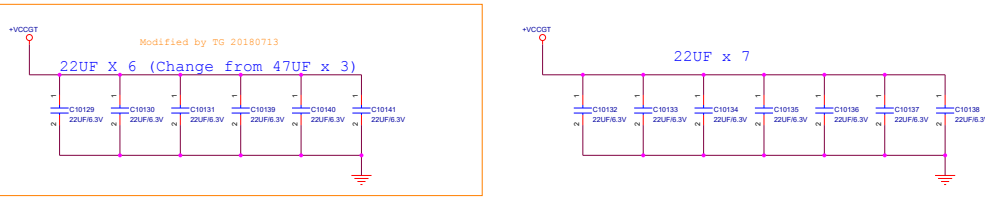
+VCCORE near CPU



+VCCGT DECAPS Place Back Side (TOP)

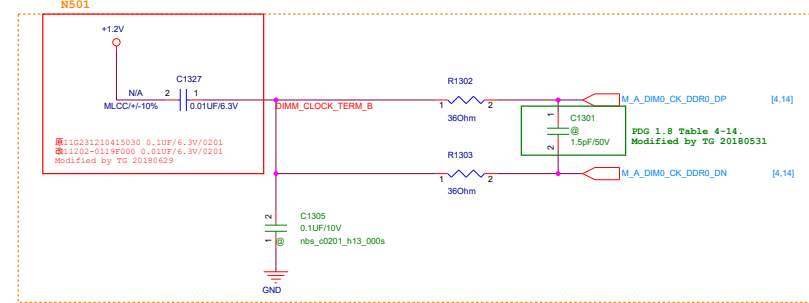
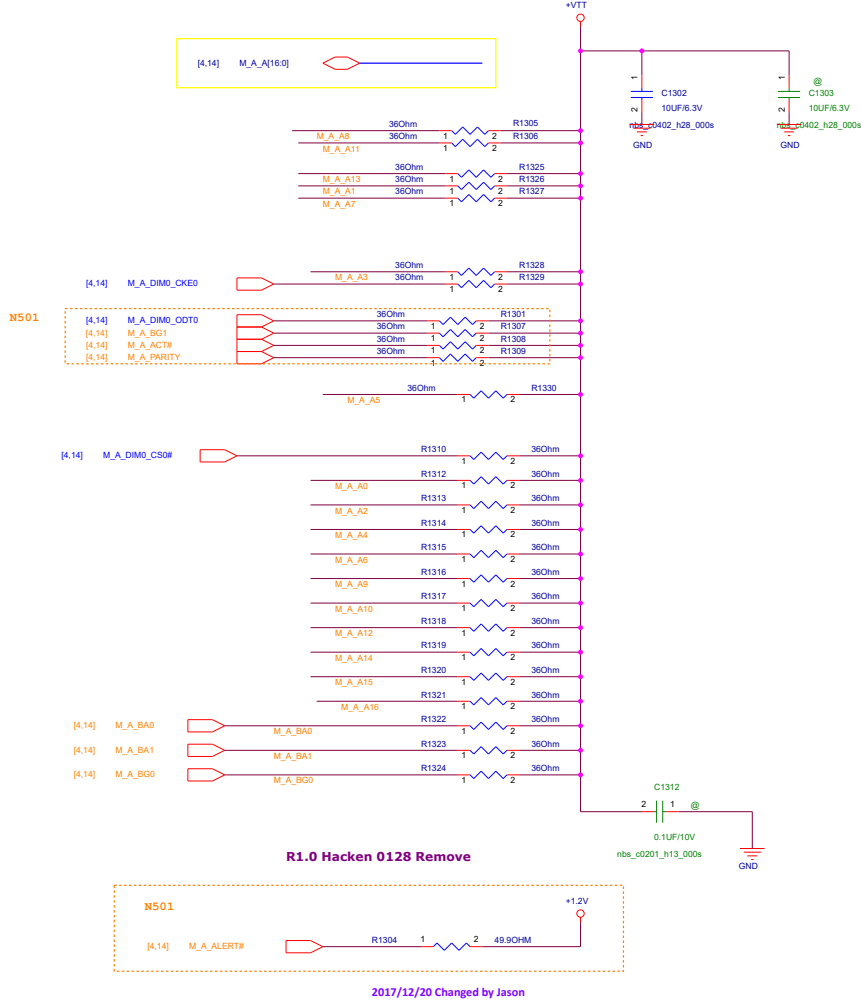


+VCCGTX near CPU



Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc _{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

		Project Name		Rev
Title :		GX502GX		R1.2
Title : TBT_Alpine-Ridge				
Issn	Dept.:	ASUSTek COMPUTER		Engineer: EE
8				
Date	Monday, February 19, 2018		Sheet	11 of 88



10uF*4
1uF*16

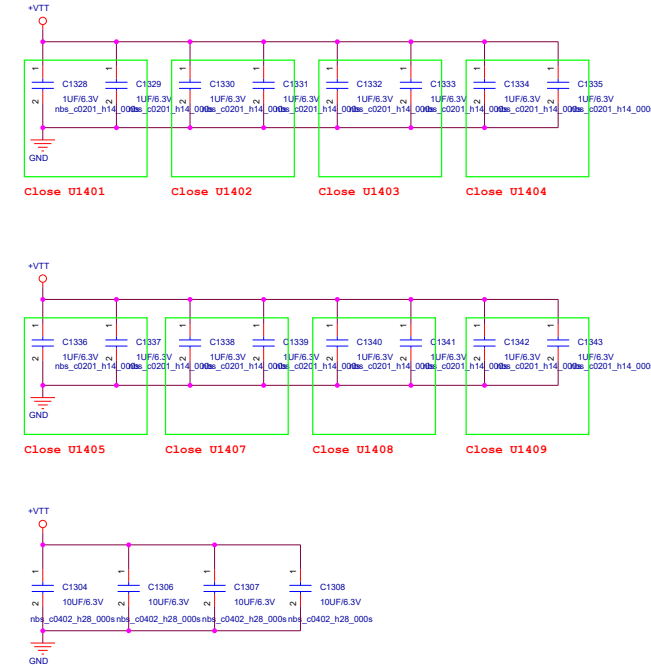


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1 μ F (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10 μ F (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1 μ F (0402)	
		Distributed around the DRAM devices	10x 10 μ F (0603)	
	VTT	Distributed along termination resistors	32x 1 μ F (0402)	
		Distributed evenly across domain	8x 10 μ F (0603)	

<Core Design>

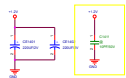
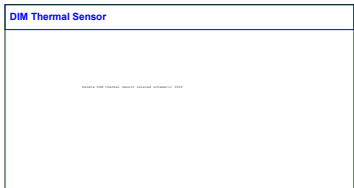
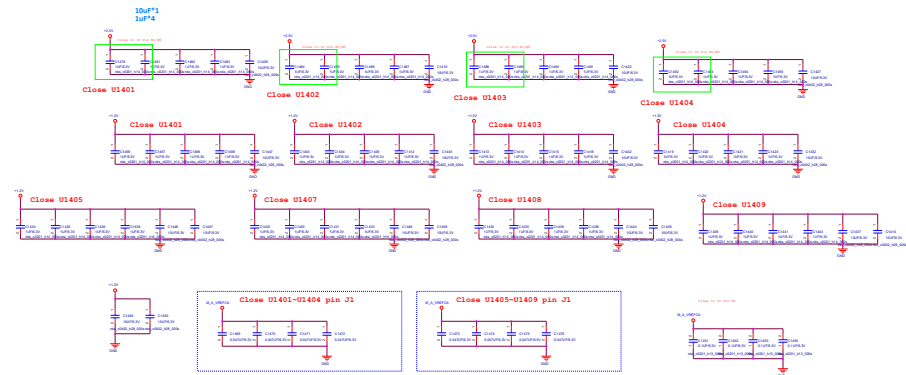
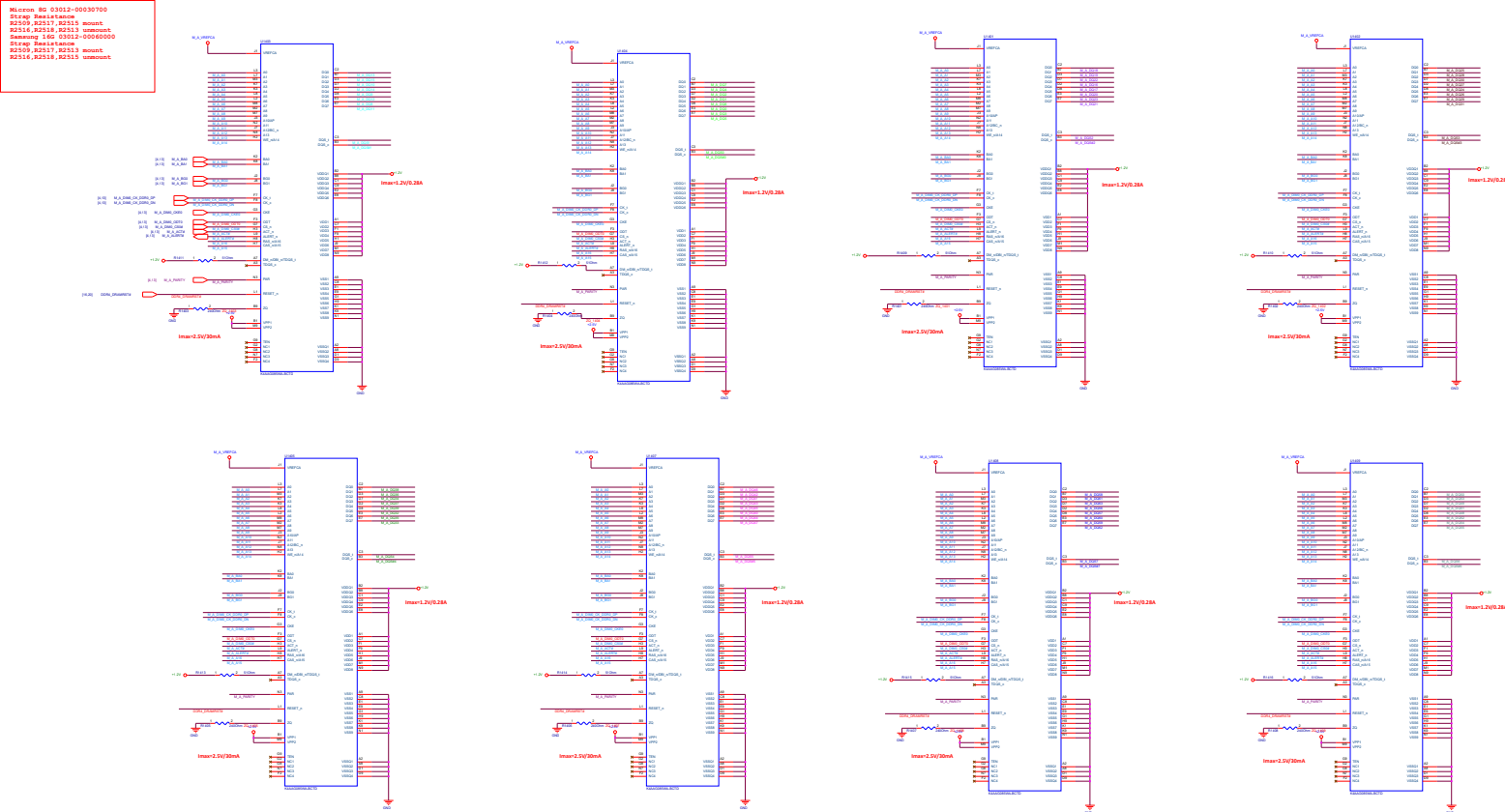



Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (Notes)	Note
DDR4 Memory Down 8B 8 Devices per Channel	VDDQ/VDD0 (Unbuffered)	4 at near each 8B DIMM device as possible Distributed around the DIMM devices (min of 4B stuffed)	44x 1µF (0603) (min of 4B stuffed)	
	VDDQ/VDD0 (Buffered)	2 at near each 8B DIMM device as possible Distributed around the DIMM devices	20x 10µF (0603) 32x 1µF (0603)	
	VTT	Distributed around the termination resistors	32x 10µF (0603) 32x 1µF (0603)	
	VTT	Distributed evenly across domain	8x 10µF (0603)	

		Title : DDR4_ON-BOARD_A2	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 15 of 99	


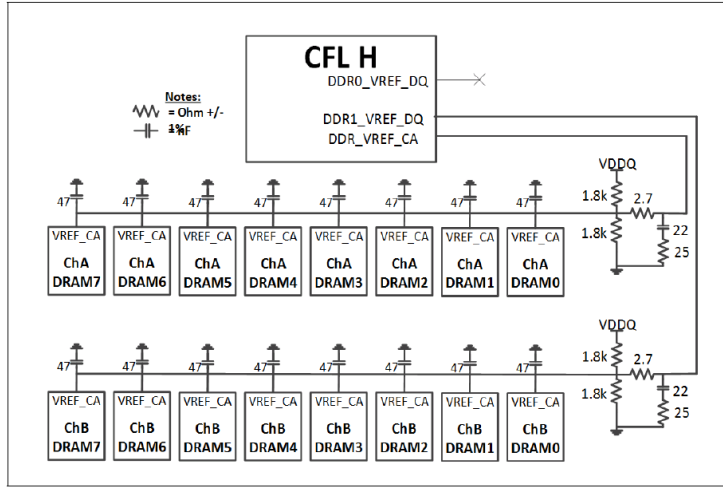
		Title : NB_****	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 17 of 99	

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



Memory Down Vref

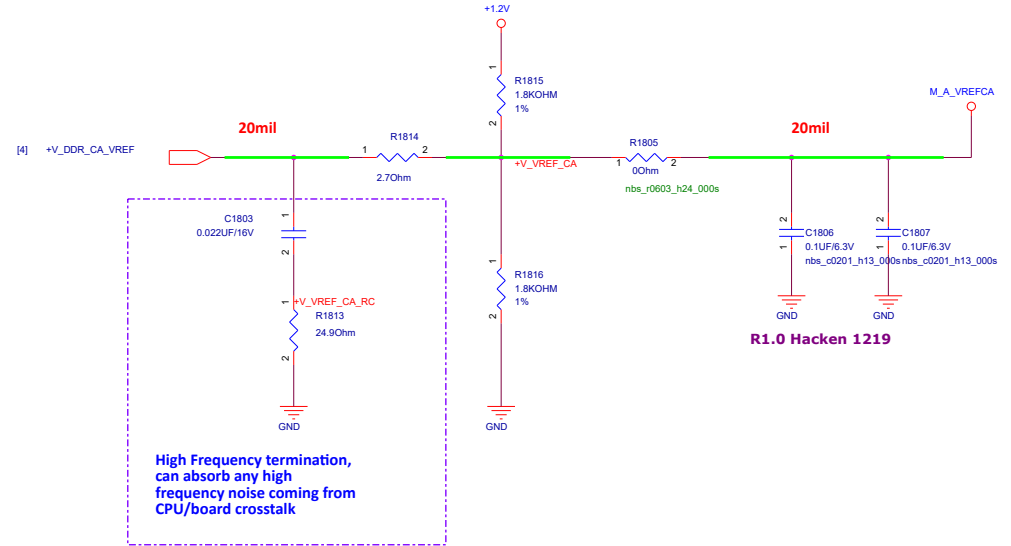
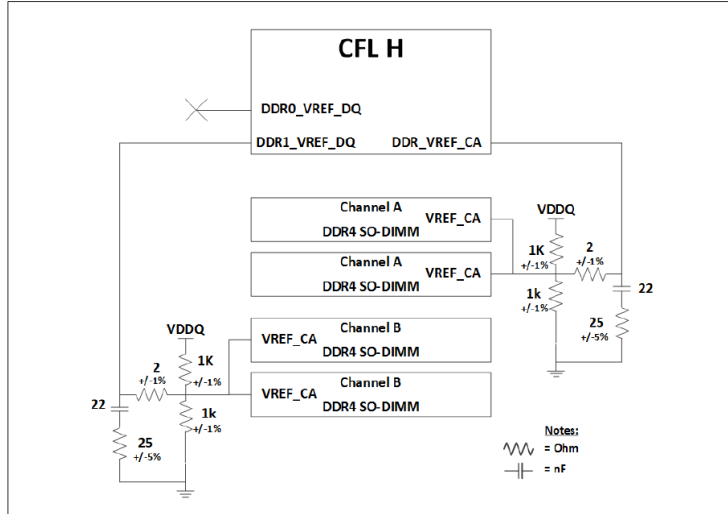
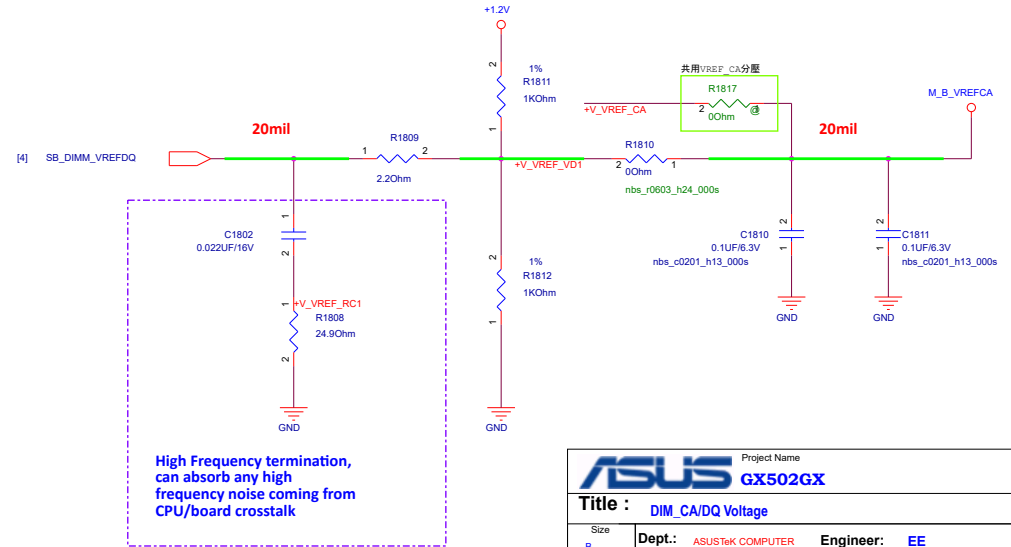



Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

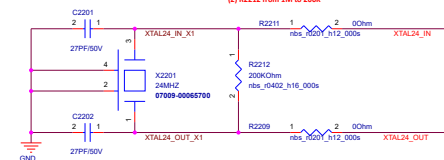


SO-DIMM1 Vref

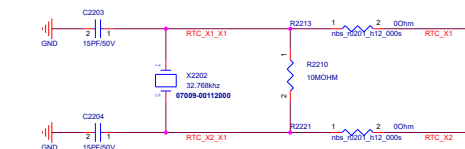


		Title : *****	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 19 of 99	

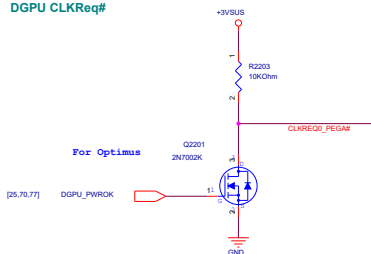
2017/12/25 Changed by James
(1) X2201 from 07009-0062000 to 07009-00065700
(2) R2212 from 1M to 200K



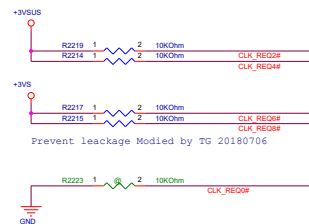
RTC CRYSTAL 32.768KHz



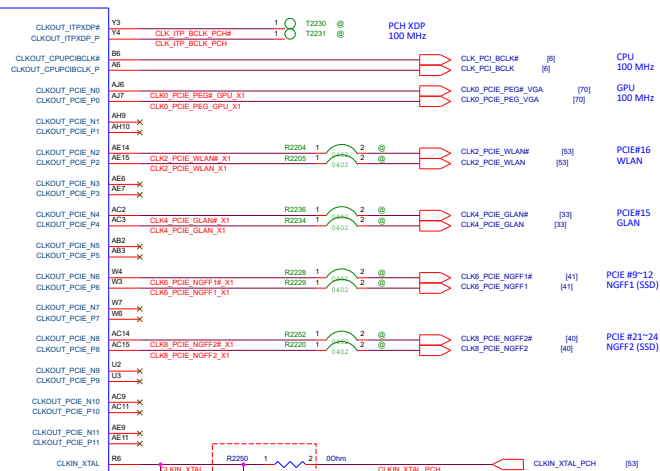
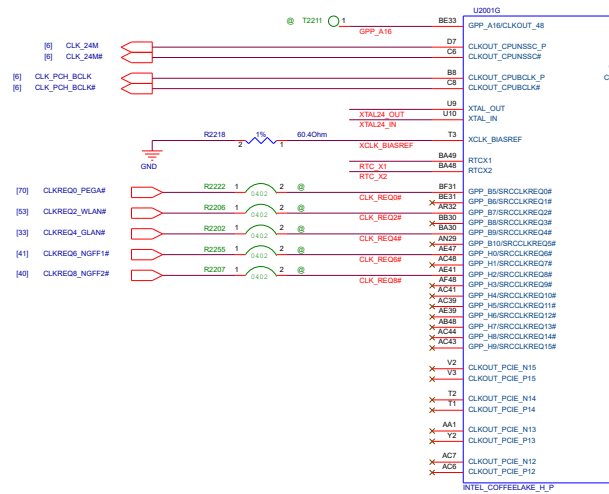
DGPU CLKReq#



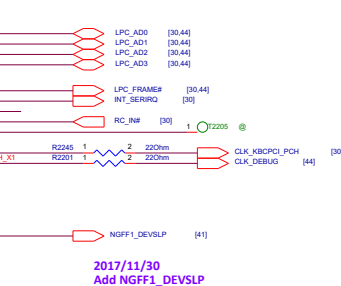
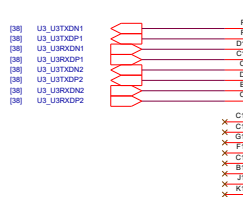
PCH CLKREQ Setting:



```
#0 : GPU
#2 : WLAN
#4 : GLAN
#6 : SSD1
#8 : SSD2
```



USB3.1 Port1 : Standard A
J3801



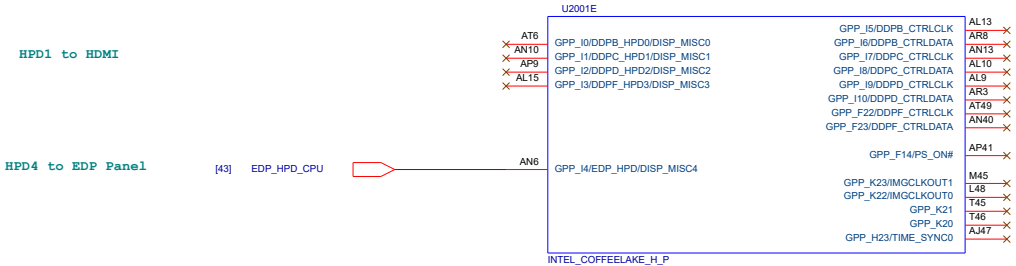
USB3.1 Port3 : Standard A
J5202



USB3.1 Port1 : Type C
I4701



- HPD0 to DP
- HPD1 to HDMI
- HPD2 to TBT
- HPD3 to VGA
- HPD4 to EDP Panel



DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected

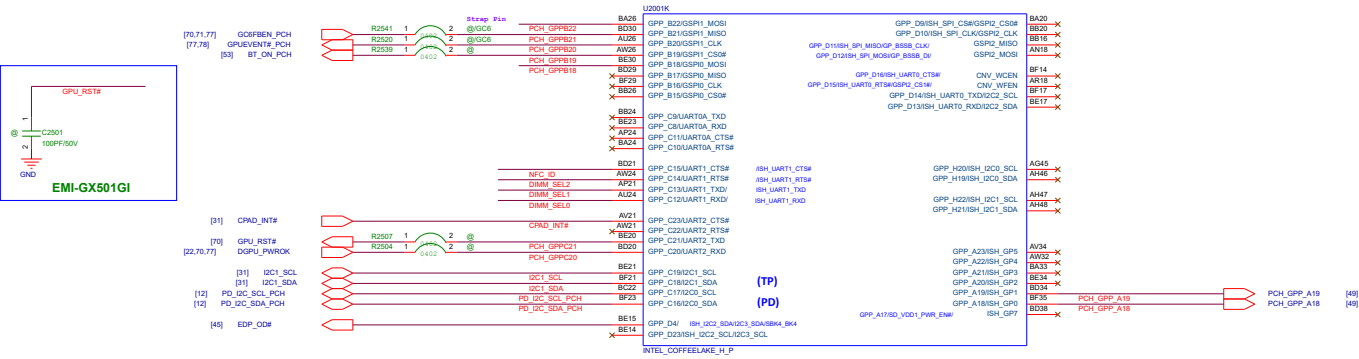
GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PCH_PWROK de-asserts.This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PCH_PWROK de-asserts.This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PCH_PWROK de-asserts.This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected.</p> <p>Notes:</p> <ol style="list-style-type: none">The internal pull-down is disabled after PCH_PWROK de-asserts.This signal is in the primary well.This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

5.6 Digital Display Interface Disabling and Termination Guidelines

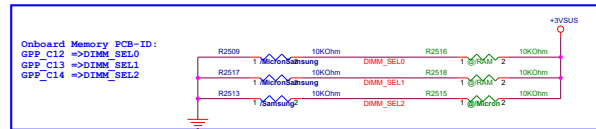
All the digital display ports on the Coffee Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

Table 5-15. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect



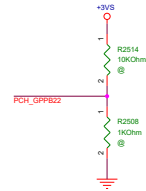
2017/12/05 Remove TBT_I2C_SCL_PCH/TBT_I2C_SDA_PCH by James



DDR4 Memory Down pool

	Micron (1Rx8Gb)	Samsung (1Rx16Gb)	
	93012-00030705 Micron DDR4 2666 MFDGA108SA-0751E	93012-00040000 Samsung DDR4 2666 MAMG0108MA-WCT0	
DIMM_SEL0	L	L	
DIMM_SEL1	L	L	
DIMM_SEL2	H	L	

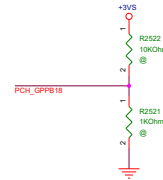
Strap => Boot BIOS Strap Bit BBS



```
PCH_GPPB22: weal internal pull down
```

PU	LPC
PD	SPI (Default)

Strap => No Reboot



NOTE: Enable No Reboot
FCM will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down

PU	Enable
PD	Disable (Default)

X-tal Frequency Select

Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Cannon Lake PCH-H

- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm $\pm 5\%$ pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

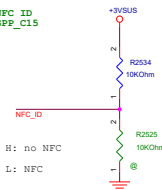
PCB ID0 GPP_D9

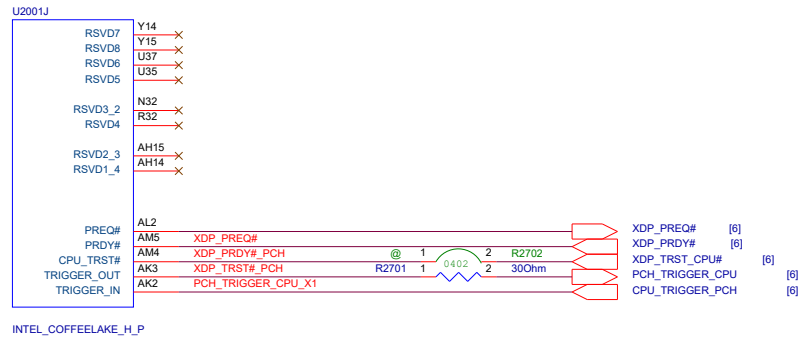
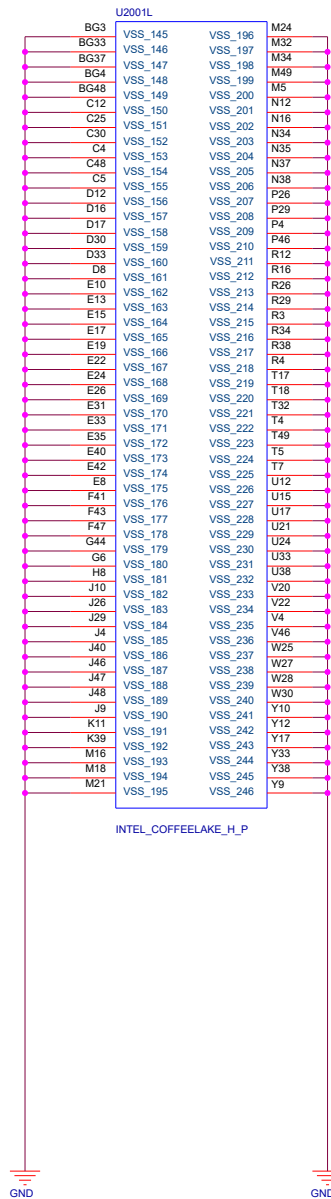
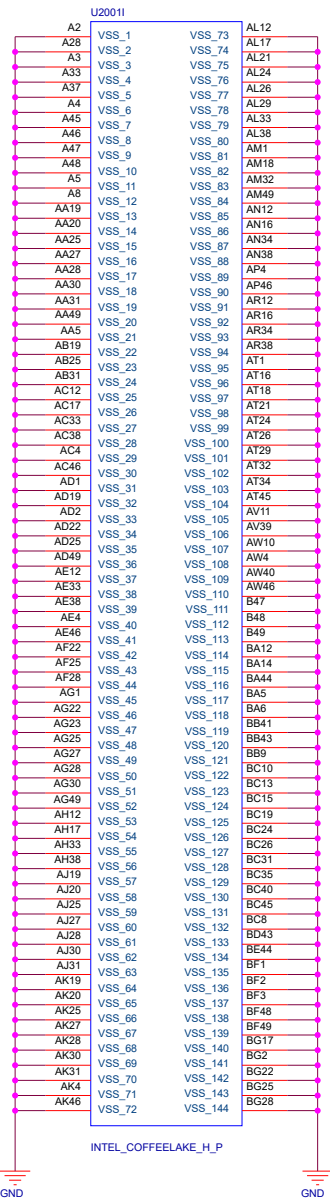
PCB ID1 GPP_D10

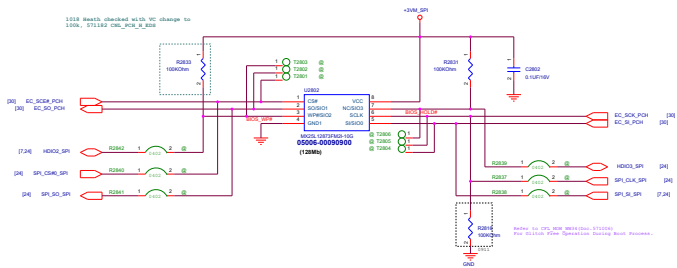
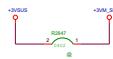
Touch Pad ID
GPP_D11

Touch Panel ID
GPP_D12

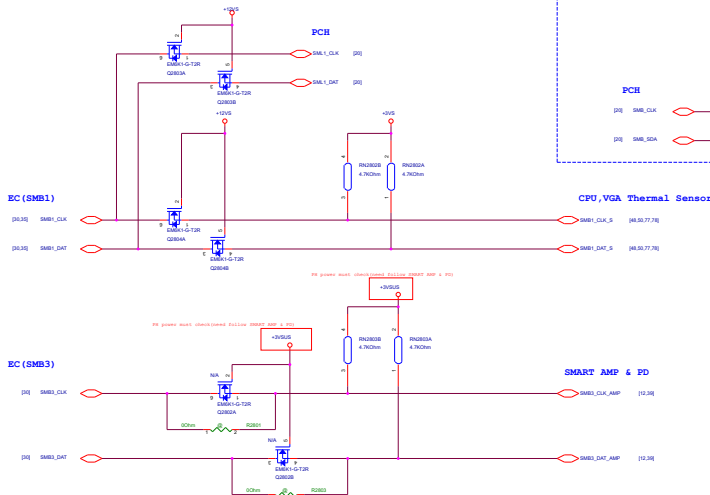
NFC ID
GPP_C15



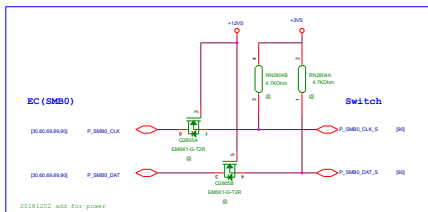
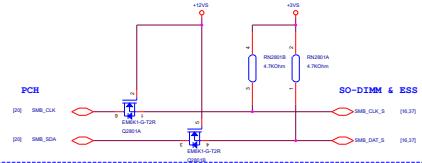





System Management Interface

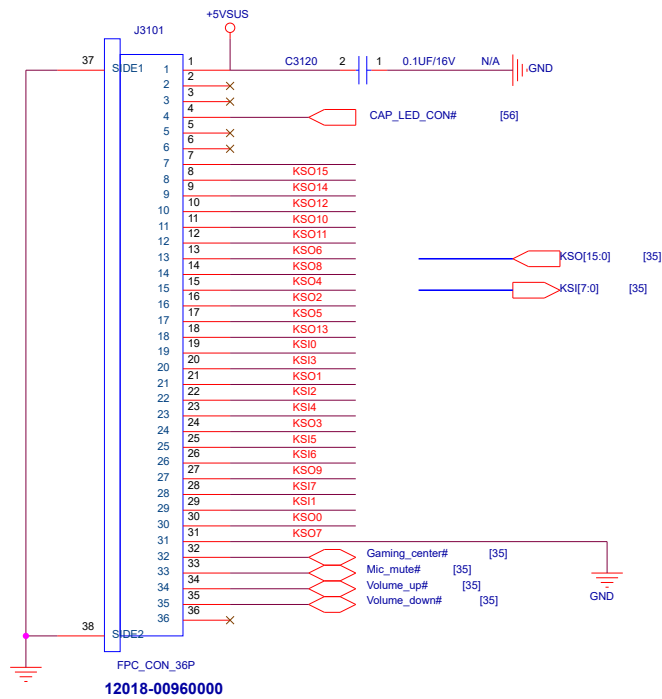


SMBus Interface

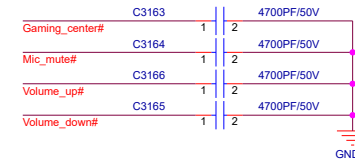
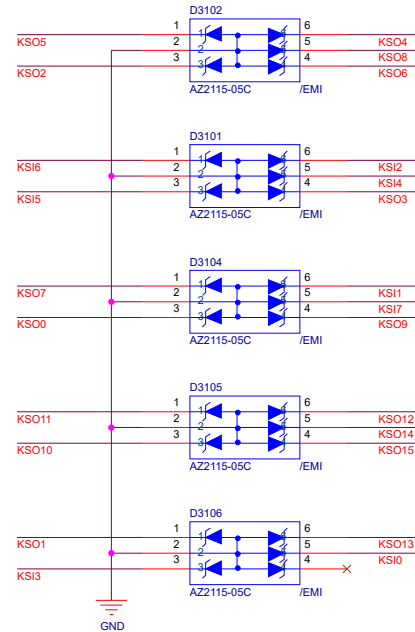


		Project Name	Rev
		GX502GX	R1.2
Title : TEST POINT			
Size B	Dept.: ASUSTeK COMPUTER	Engineer:	EE
Date: Monday, February 18, 2019	Sheet	29	of 99

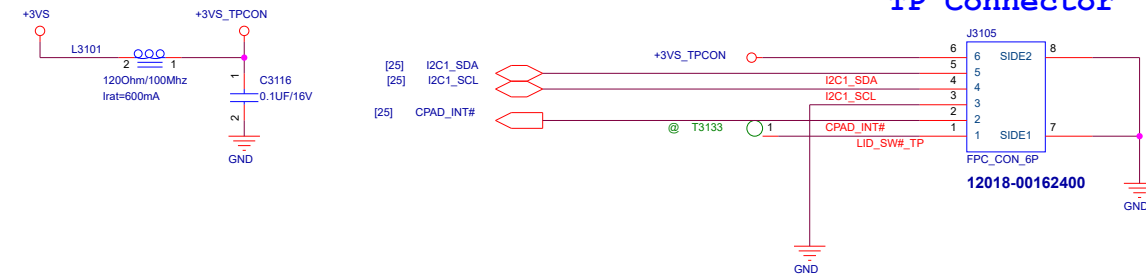
Keyboard Connector



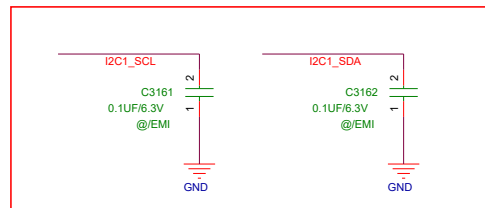
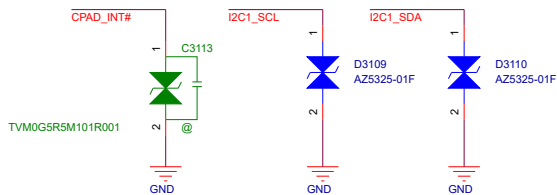
For EMI



TP Connector



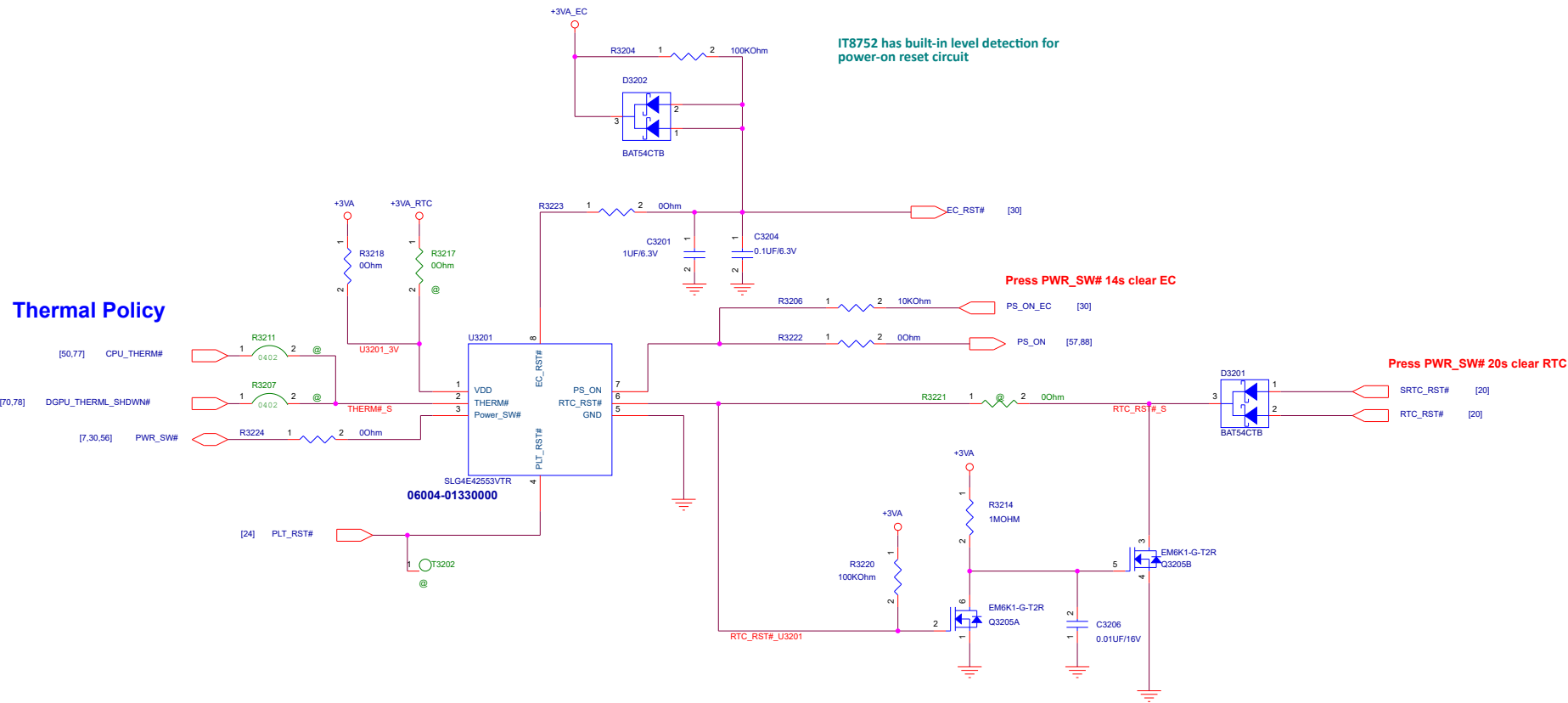
EMI Reserve
如要上件請確認容值(選擇Pico等級)




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<Core Design>

ASUS		Title : KBC_KB & TP	
ASUSTeK COMPUTER		Engineer: EE	
Size	Project Name	GX502GX	
Custom		Rev R1.2	
Date:	Monday, February 18, 2019	Sheet	31 of 99

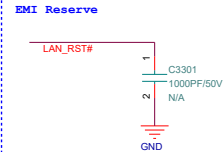
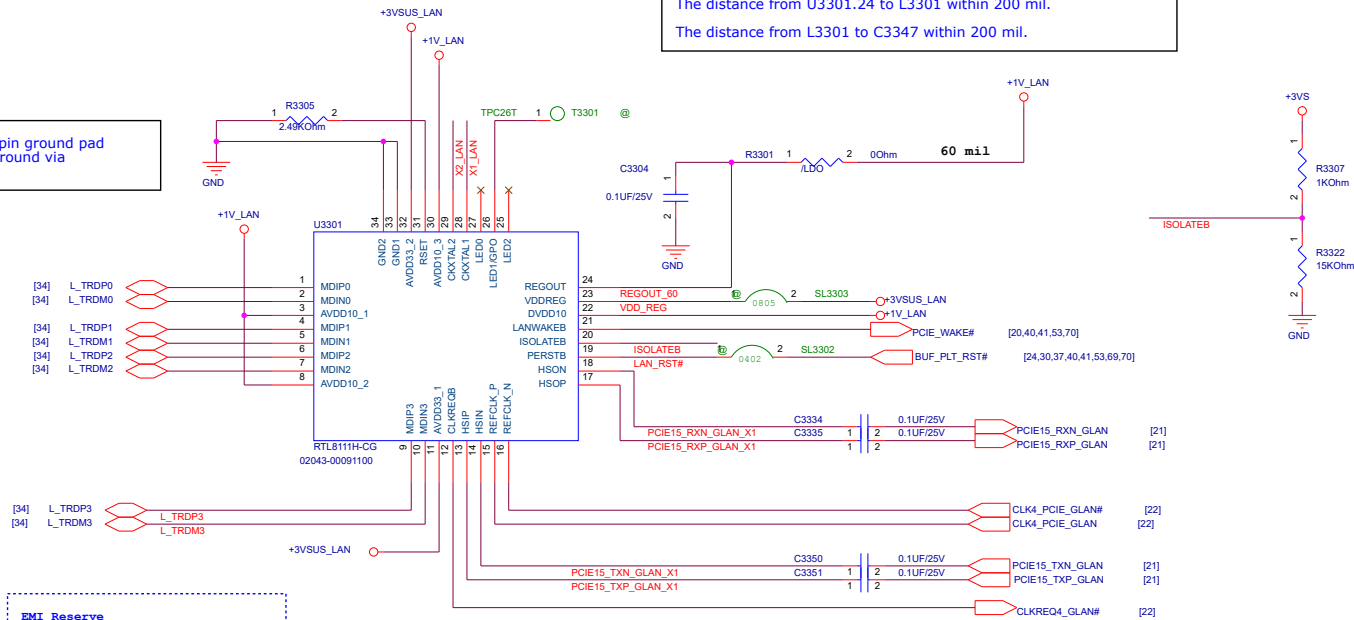


<Core Design>

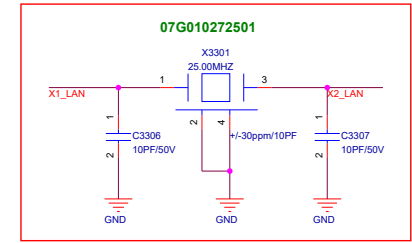
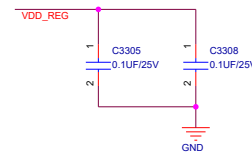
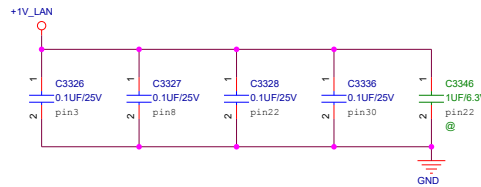
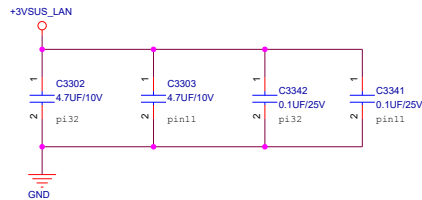
		Title : RST_Reset Circuit	
ASUSTeK COMPUTER		Engineer: EE	
Size Custom	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019	Sheet	32 of	99

33/34 pin ground pad
need ground via

The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.



CLKREQ4_GLAN#, PCIE_WAKE#
should be PU on the host side

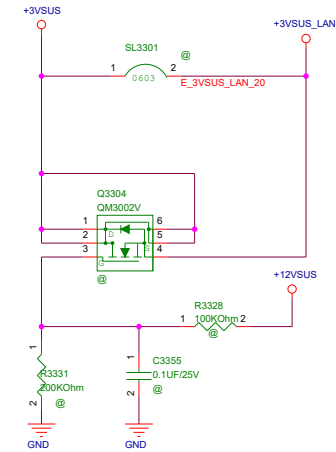


X3301: 25MHz +/-30ppm/10pF (3225)

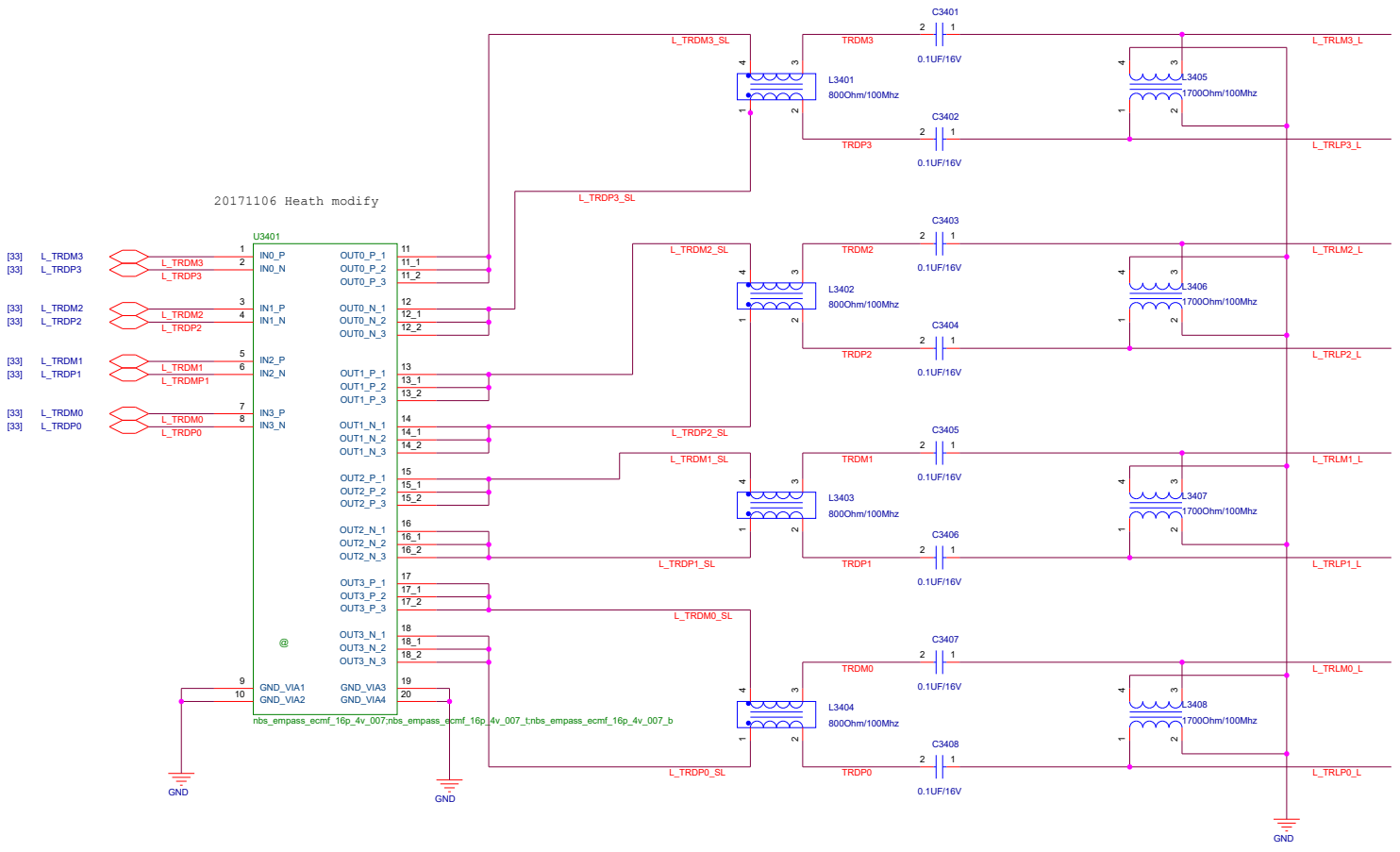
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

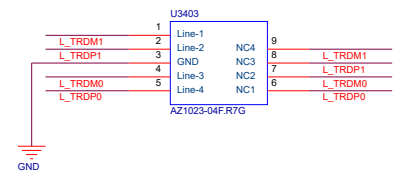
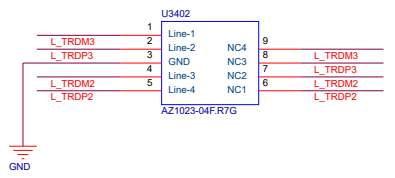
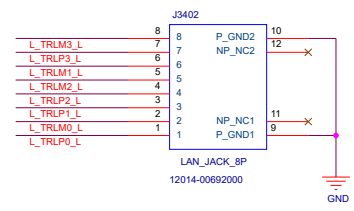
Realtek suggests 3V_LAN raise time >1ms



20171106 Heath modify



LAN Connector

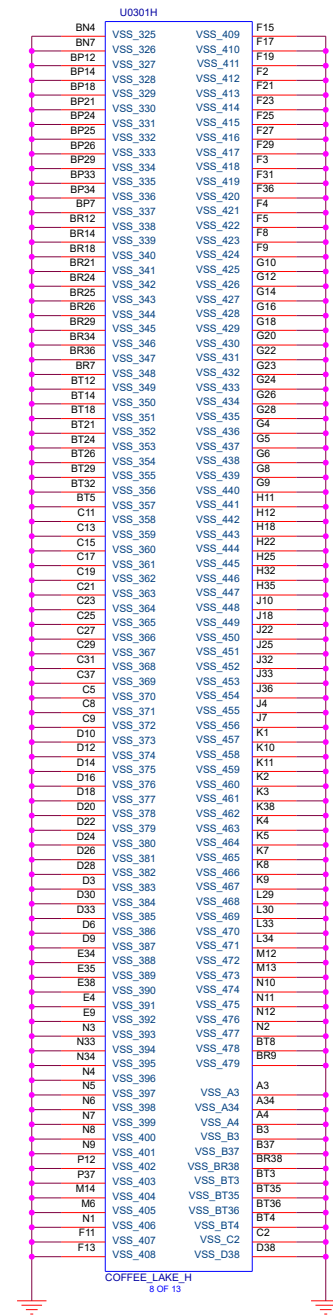
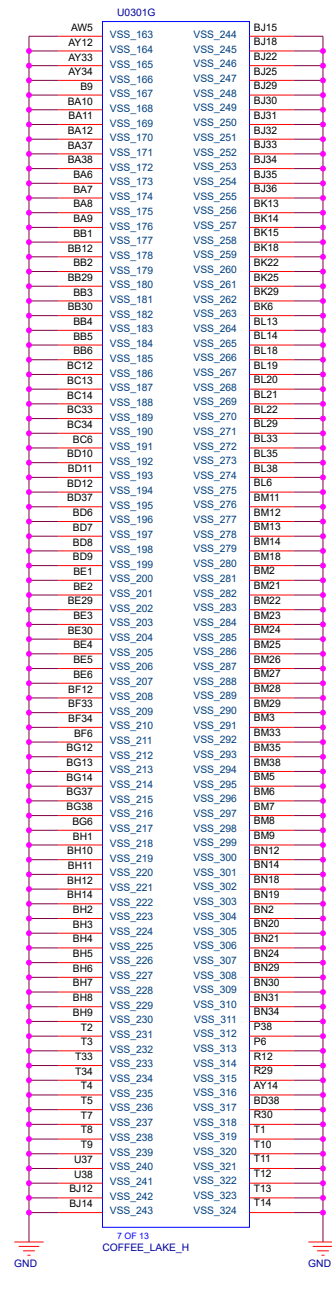
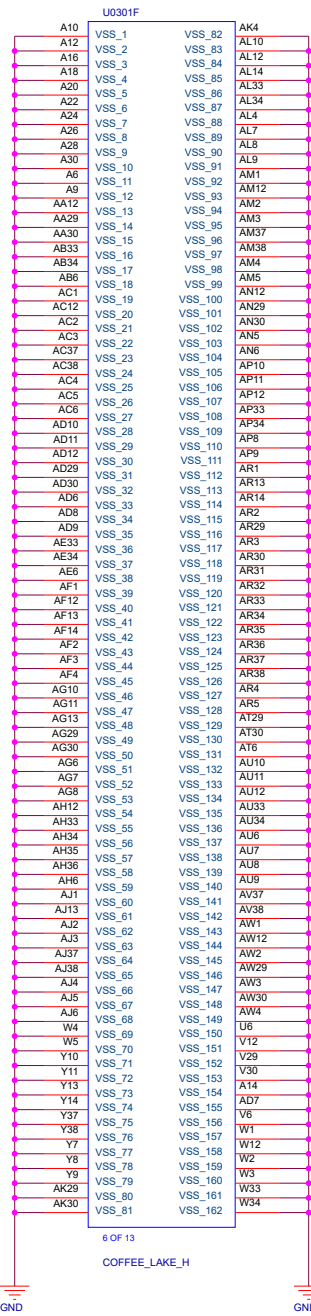


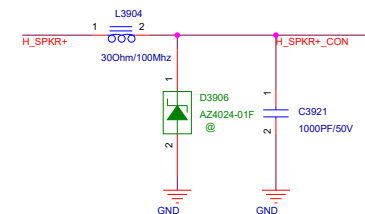
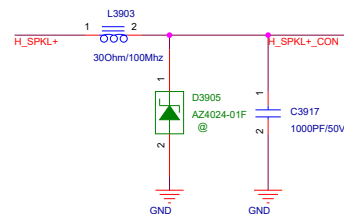
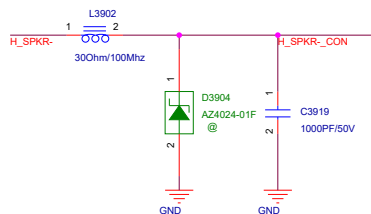
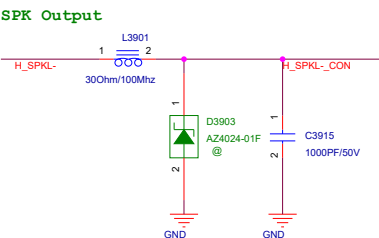
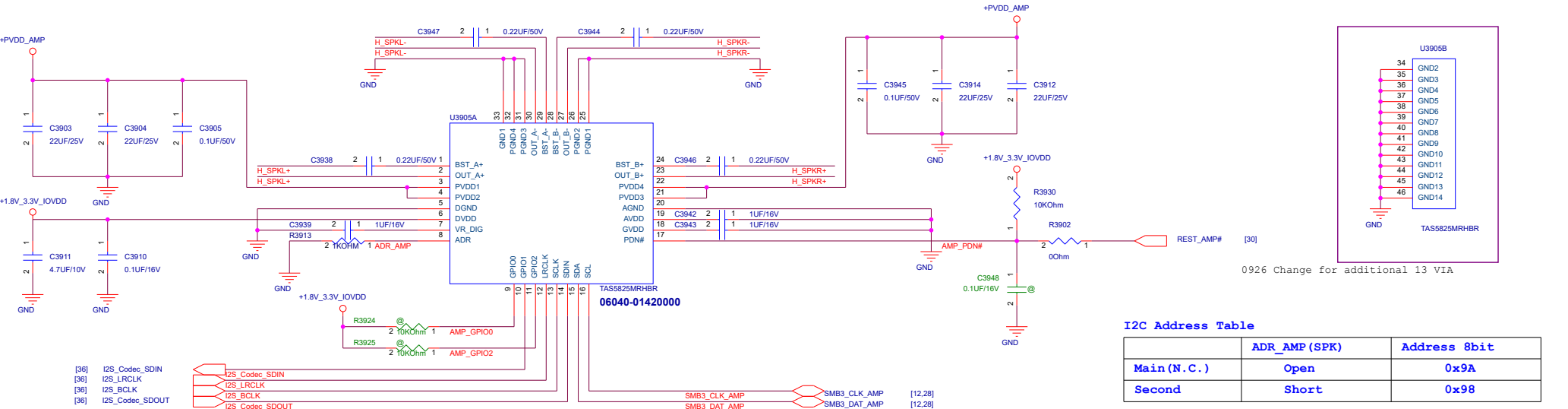
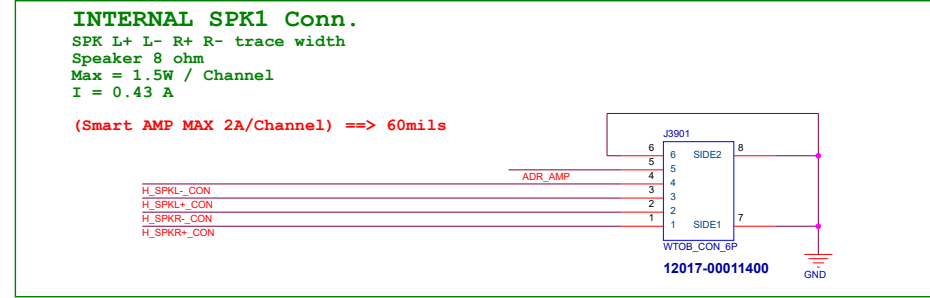
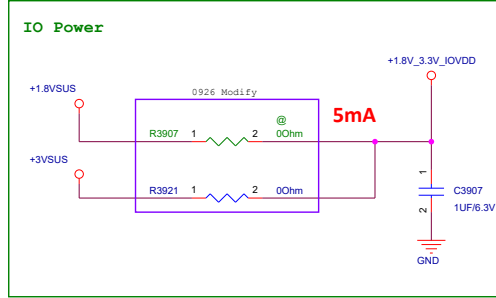
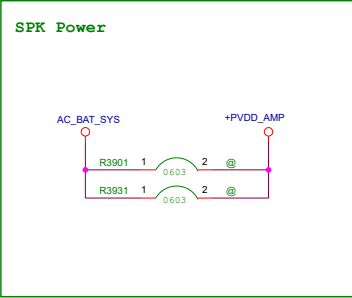
D3401,D3402 ESD Diode

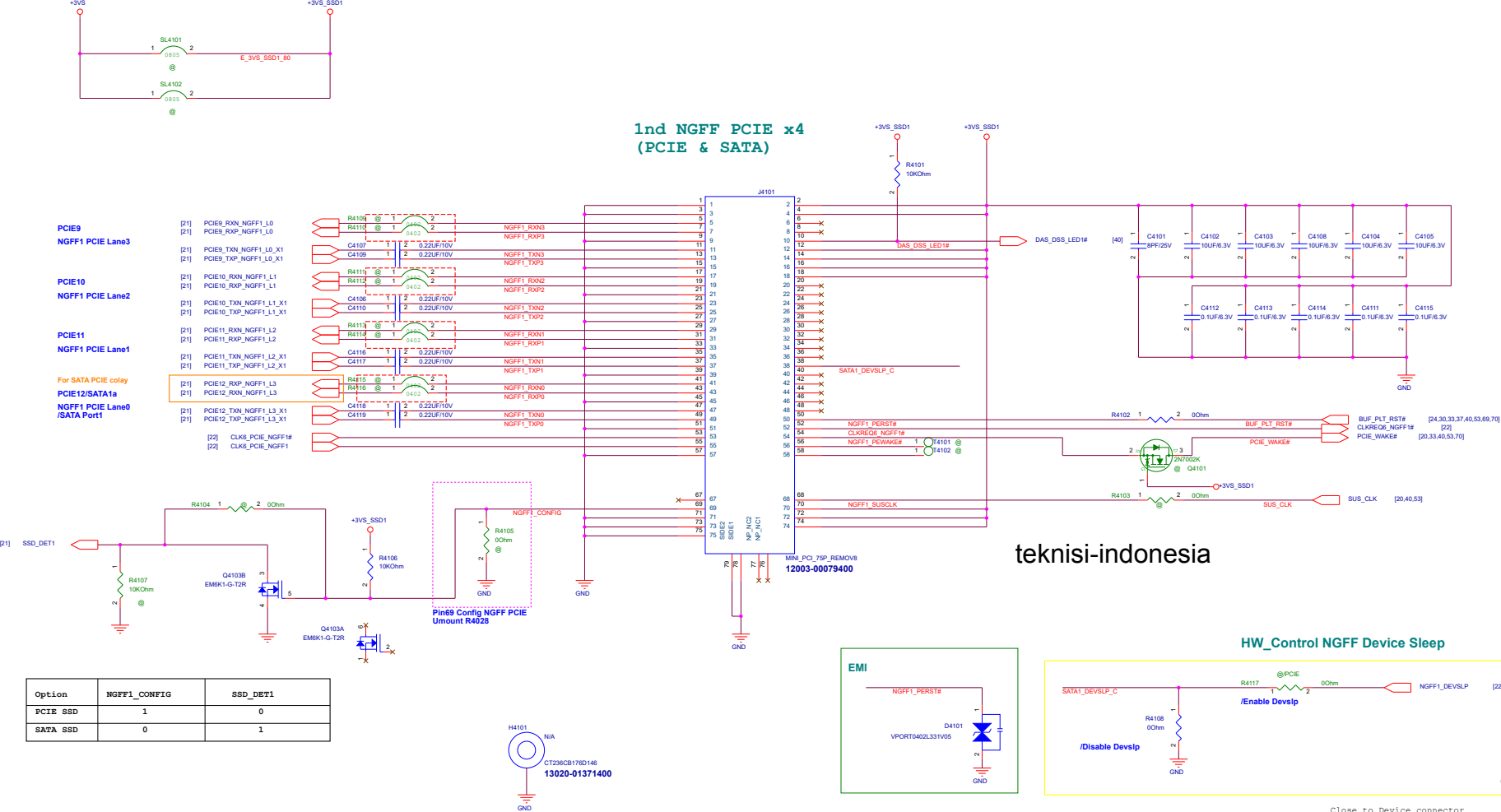
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D


Project Name		Rev
ASUS GX502GX		R1.2
Title : LAN_RJ45_CON		
Size	Dept.: ASUSTeK COMPUTER	Engineer: EE
B	Date: Monday, February 18, 2019	Sheet 34 of 99





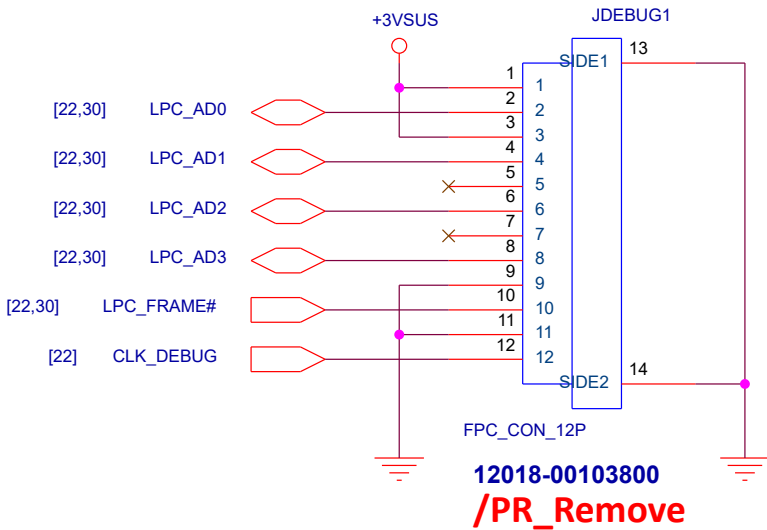


<Core Design>

		Title : XDD_HDD & ODD CON	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 42 of 99	

LPC Debug Port

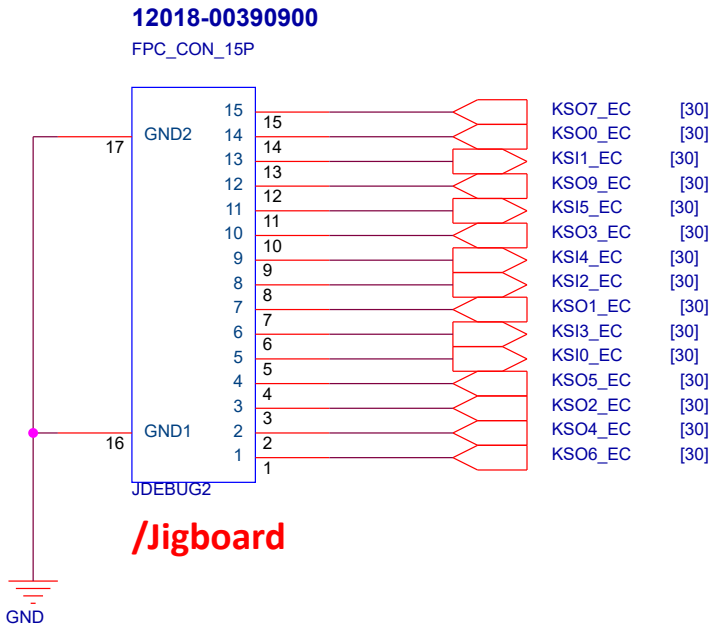
2017/11/10




1st: 12018-00103800
2nd :12018-00103300

2017/11/10

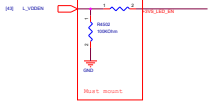
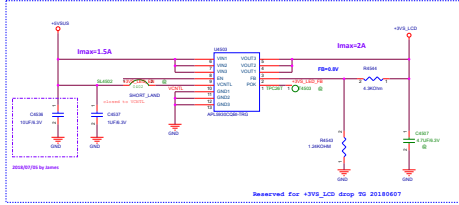
Flash BIOS



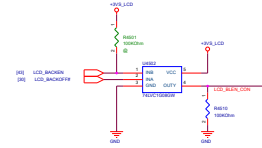
<Core Design>

		Title : DEBUG_LPC	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 44	of 99

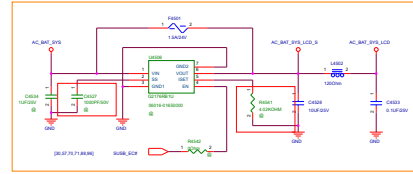
LCD Power switch



eDP_BLEN

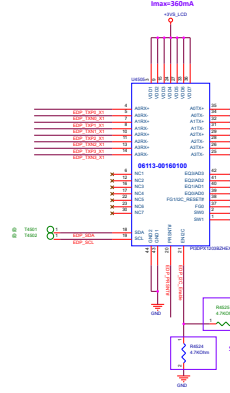
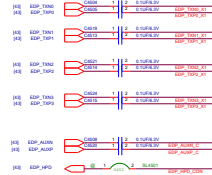


Panel BL Power

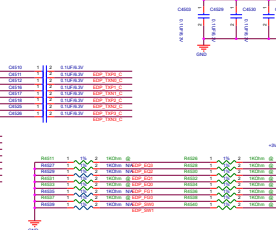


Q753Y1 Mouser

eDP from CPU



EDP1.4 Re-driver

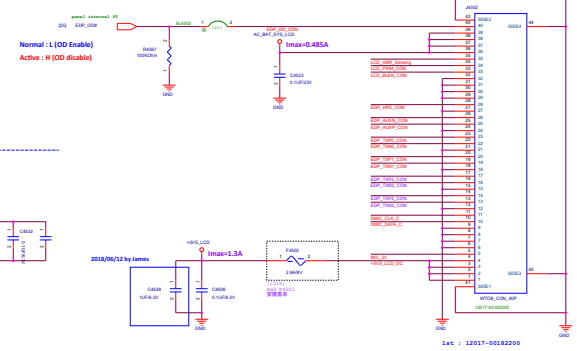


First Data Control - relation bits for the 00 value.
Read Device - control the intensity of the output signal.
00 control - select the equalization with data link channel.

Schumi (20180509)



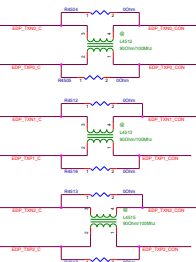
eDP Panel Conn.



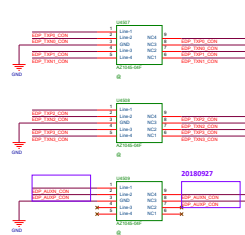
Panel Vender : AUO
PN : B156HAN02.2(HW_2A)

Pin No.	Symbol	Pin No.	Symbol
1	NC	24	LED GND
2	H_GND	25	LED GND
3	case3_N	26	LED GND
4	case3_P	27	HPD
5	H_GND	28	BL GND
6	case2_N	29	BL GND
7	case2_P	30	BL GND
8	H_GND	31	BL GND
9	case1_N	32	BL Enable
10	case1_P	33	BL PWM DIM
11	H_GND	34	NC
12	case0_N	35	NC
13	case0_P	36	BL PWR
14	H_GND	37	BL PWR
15	AUX_CH_N	38	BL PWR
16	AUX_CH_P	39	BL PWR
17	H_GND	40	NC
18	CD_VCC		
19	CD_VCC		
20	CD_VCC		
21	CD_VCC		
22	CD_Self_Test		
23	CD_GND		

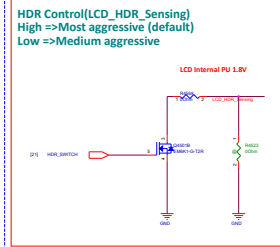
For EMI



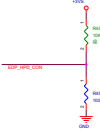
For ESD



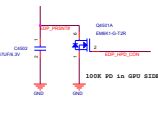
20181204(HOR Panel Pin4 Use)



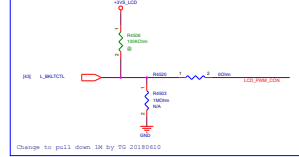
eDP_HPDC (CPU)



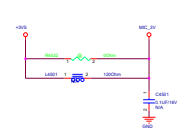
Cable Detect



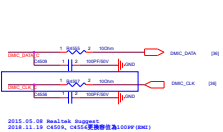
eDP_BL PWM



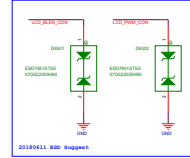
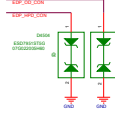
MIC module




MIC



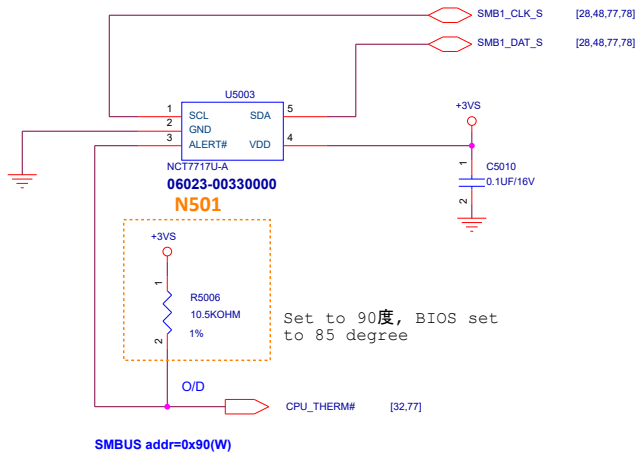
For ESD



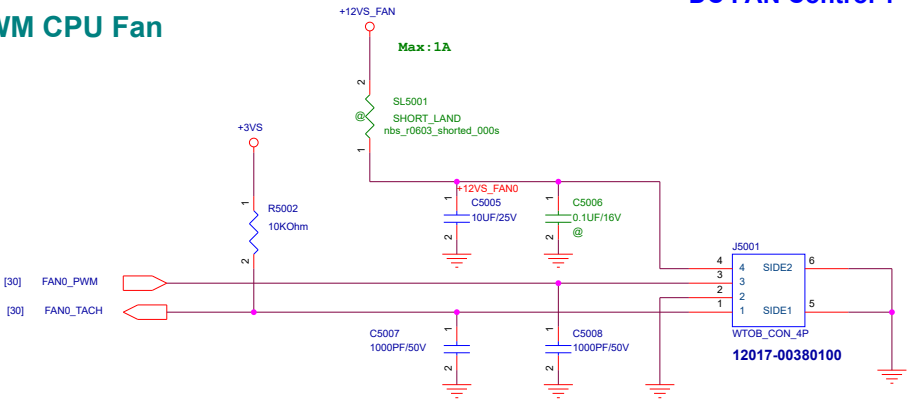
ASUS

		Title : USB3_*****	
ASUSTeK COMPUTER		Engineer: EE	
Size B	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 46 of 99	

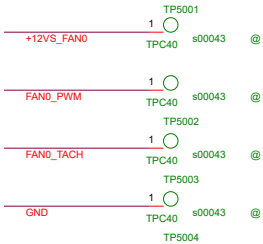
CPU Thermal Sensor



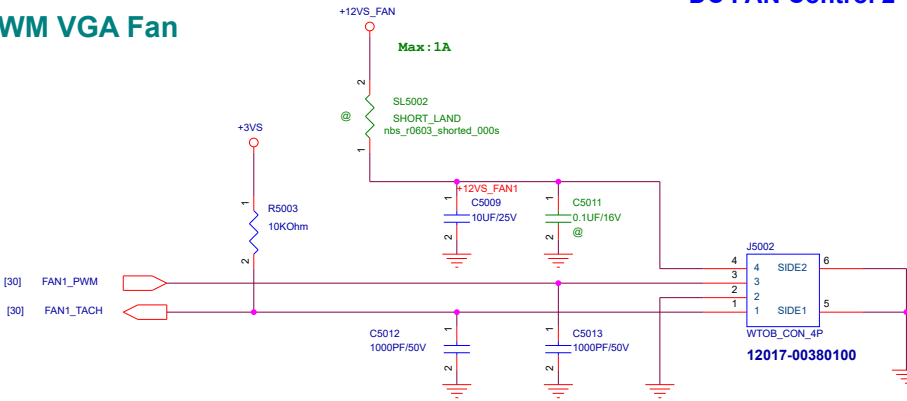
PWM CPU Fan



DC FAN Control 1



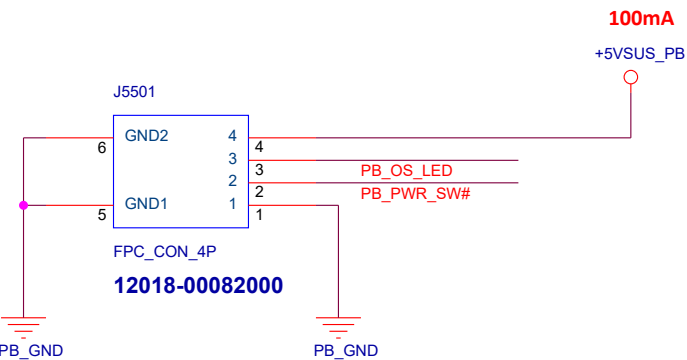
PWM VGA Fan



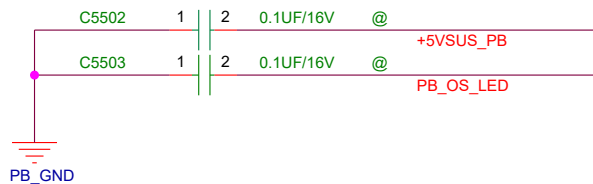
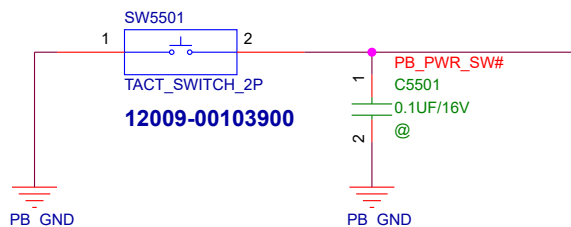
DC FAN Control 2

<Core Design>

Title <Title>		
Size A	Document Number <Doc>	Rev R1.2
Date:	Monday, February 18, 2019	Sheet 54 of 99

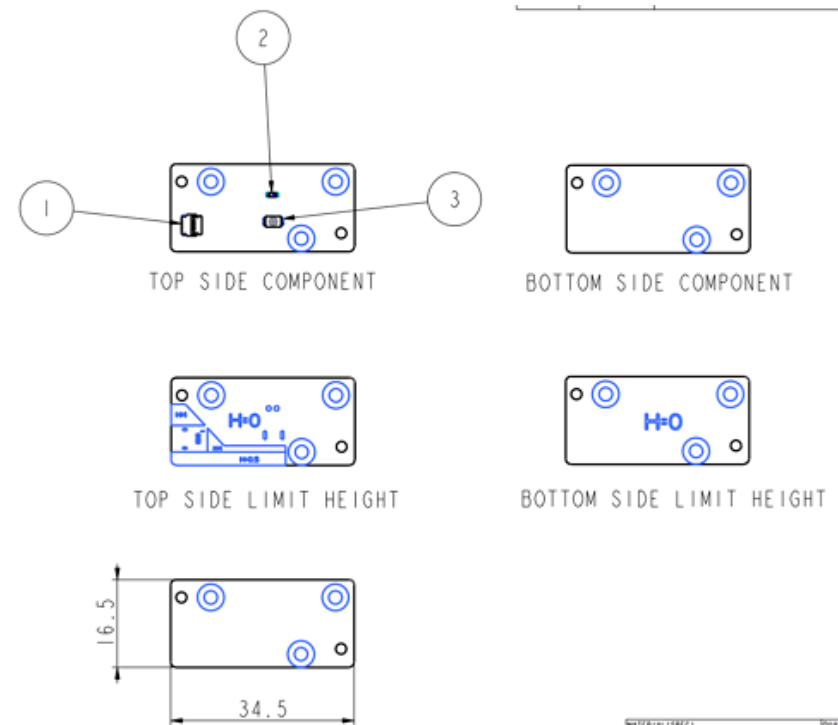
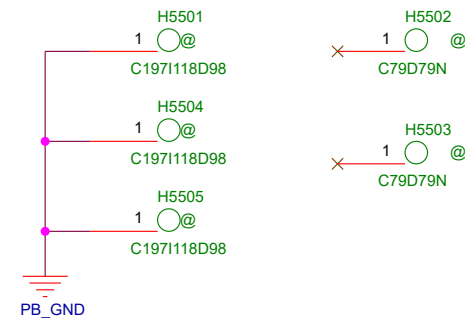
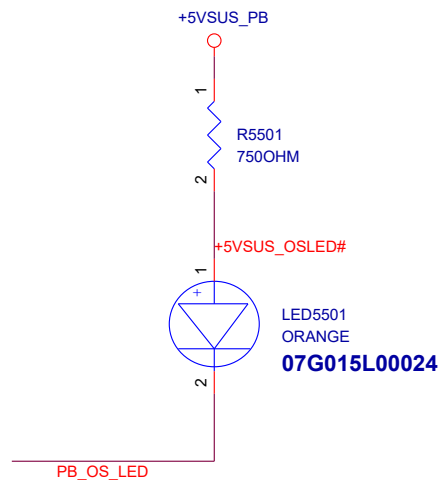


POWER button



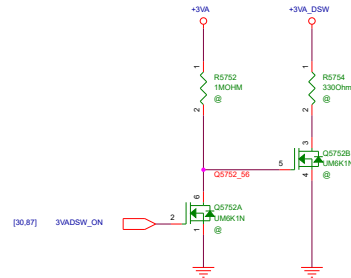
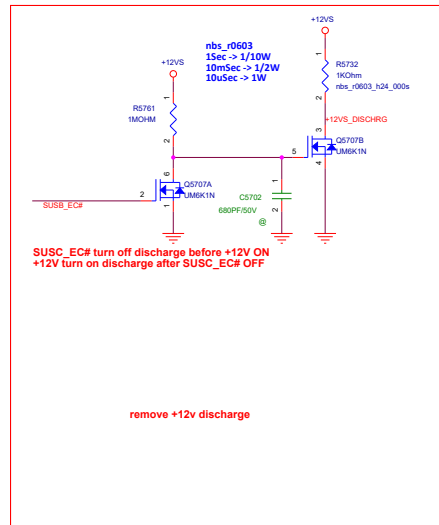
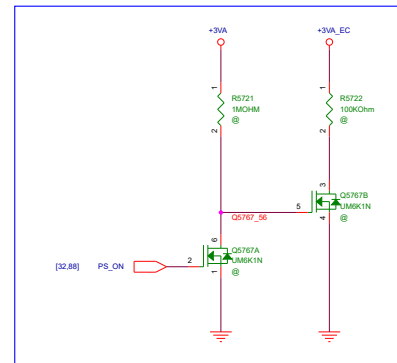
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OS LED



<Core Design>

ASUS		Title : IO Con. to MB	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019	Sheet 55	of 99	

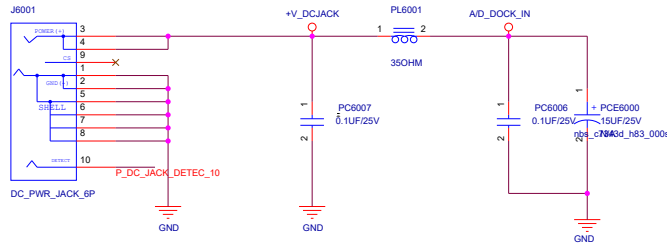


		Title : I/O_Main board Conn.	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 59 of 99	

DC-IN Connector

DC Jack使用請詢用River_Hsu

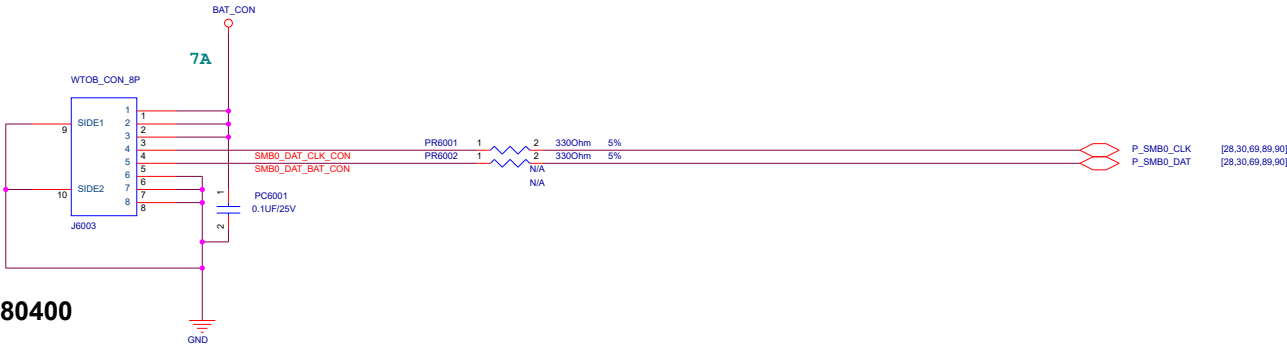
New 6 Phi 4 Pin DC_Jack 1.55ch



12033-00020300

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector




12017-00080400


Note:Battery Connector 正確性與BAT1_IN_OC#是否預留！


Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	


Plug HW Throttle(in)


POP window


		Title : BT_Blueetooth	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 61 of 99	

		Title : I/O board(1-1)_CR_RTS5139	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 62 of 99	

		Title : USB Port	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 63 of 99	

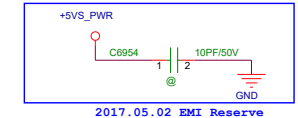
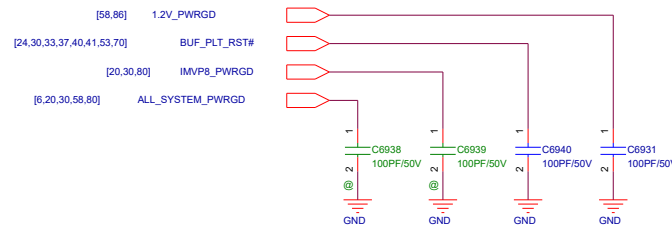
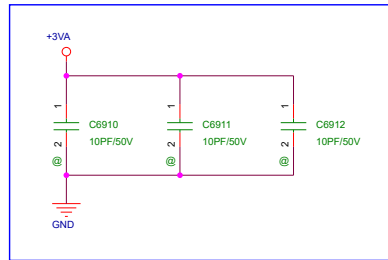
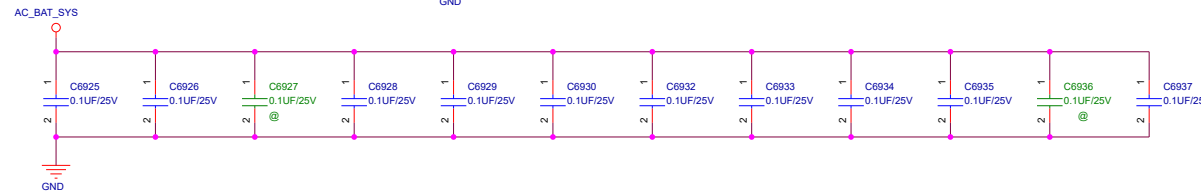
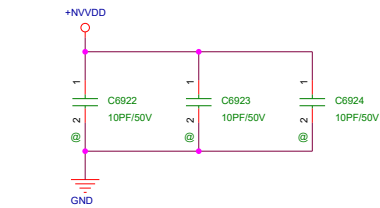
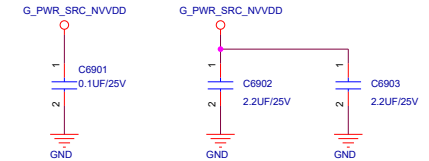
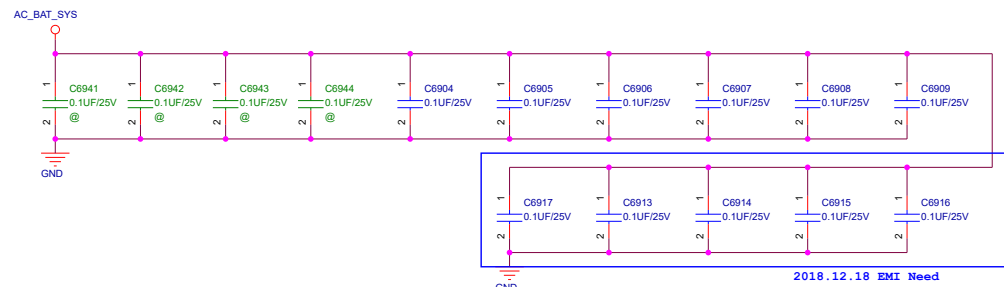
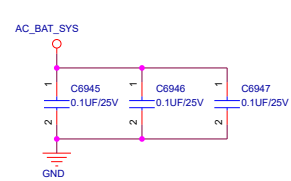
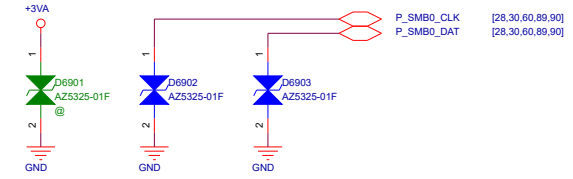
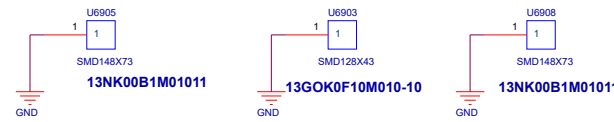
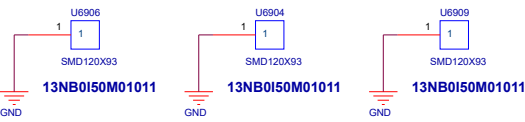
		Title : ME_Screw Hole & Nut	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 65 of 99	

		Title :	
ASUSTeK COMPUTER		Engineer:	EE
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 66 of 99	

		Title : OTH_for test only	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 68 of 99	

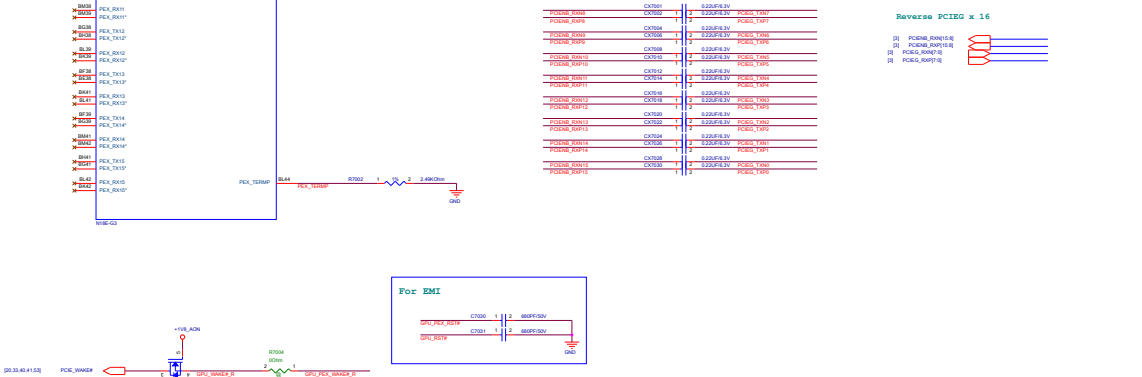
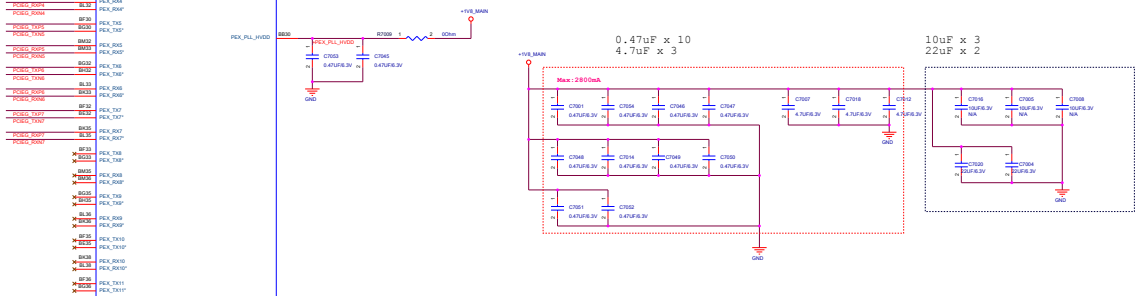
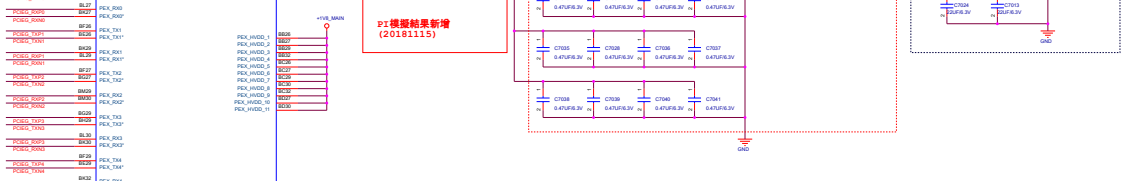
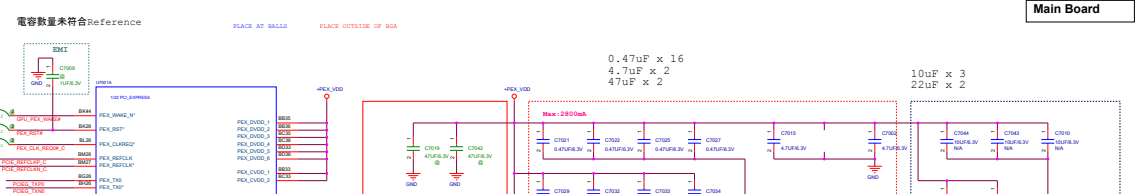
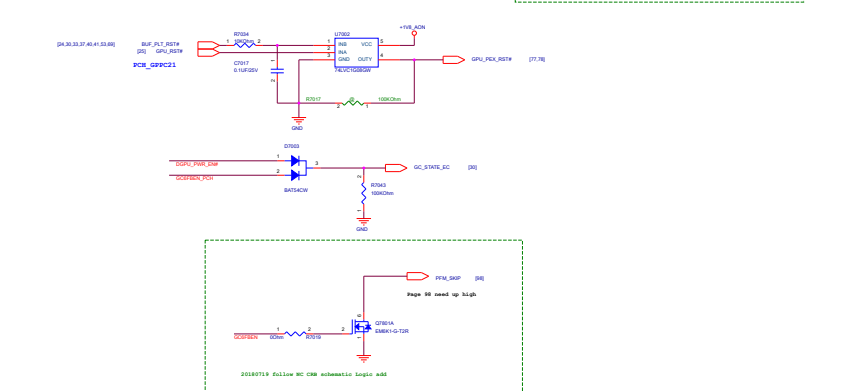
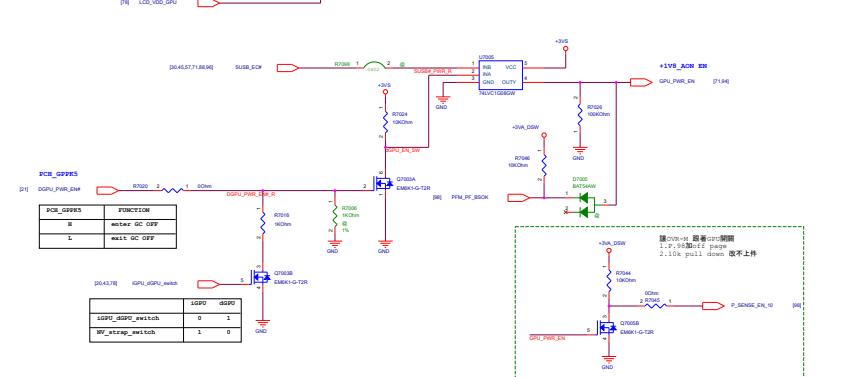
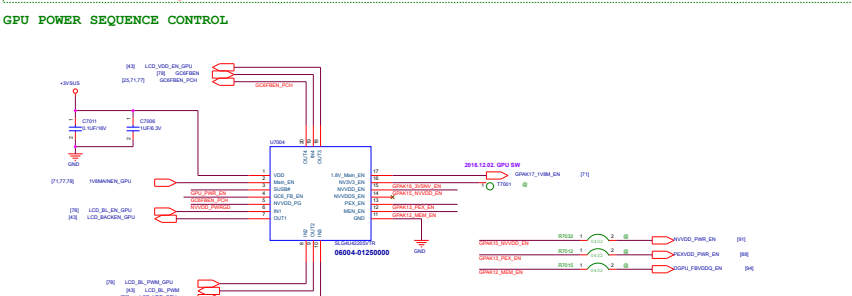
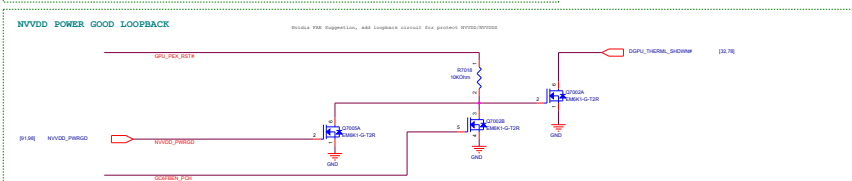
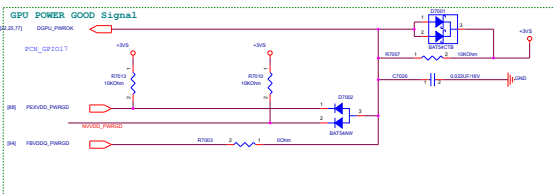
SPRING (2.6H)*3 13NB0I50M01011

EMI SPRING (4.2H)*2 13NK00B1M01011
EMI SPRING (3.5H)*1 13GOK0F10M010-10

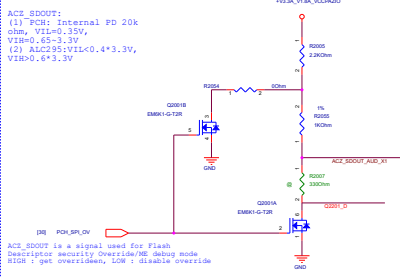
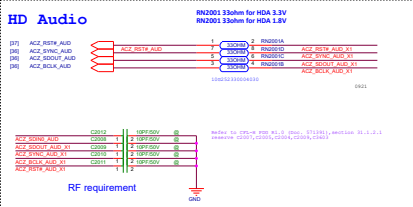


2018.11.19 EMI Reserve

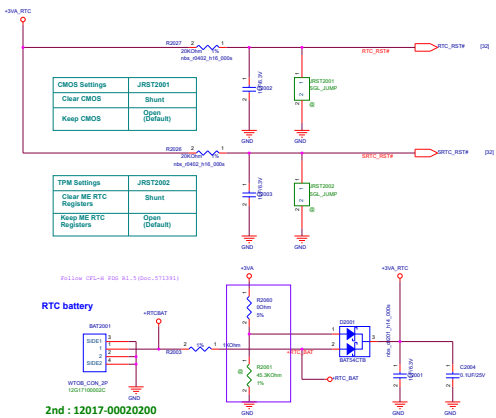
<Core Design>



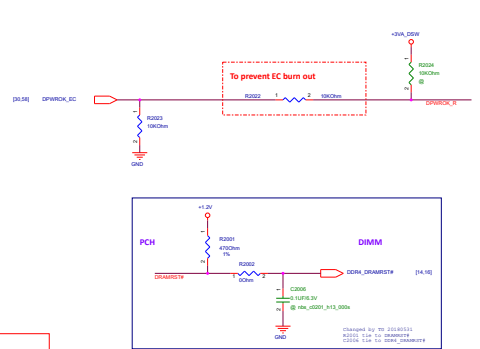
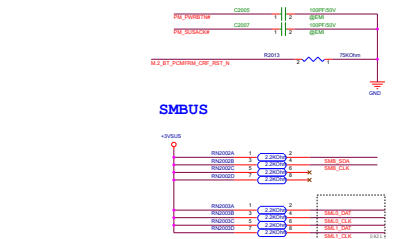
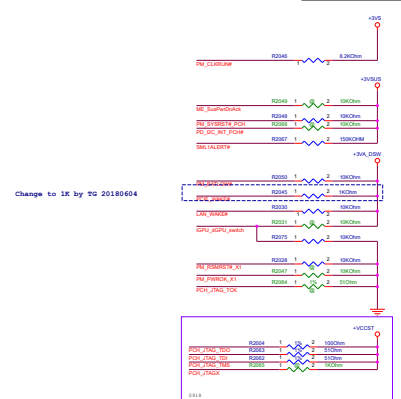
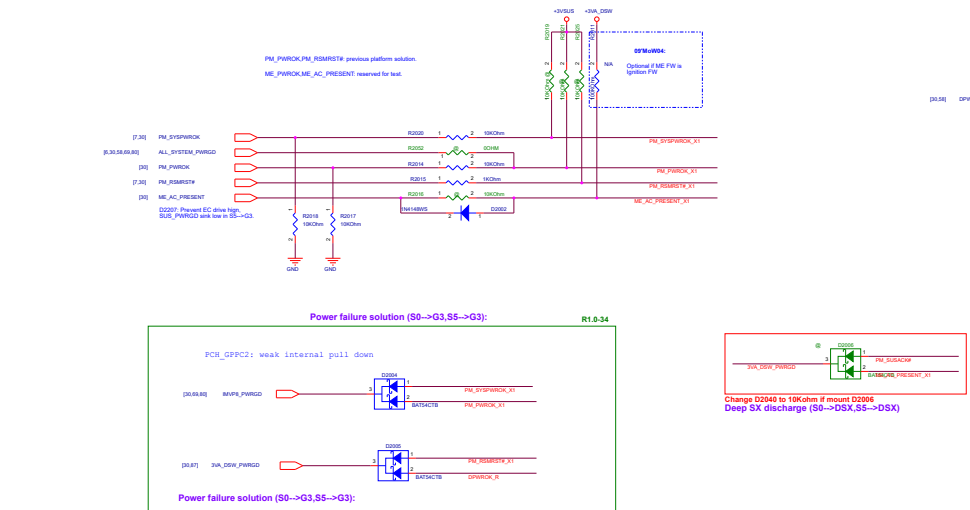
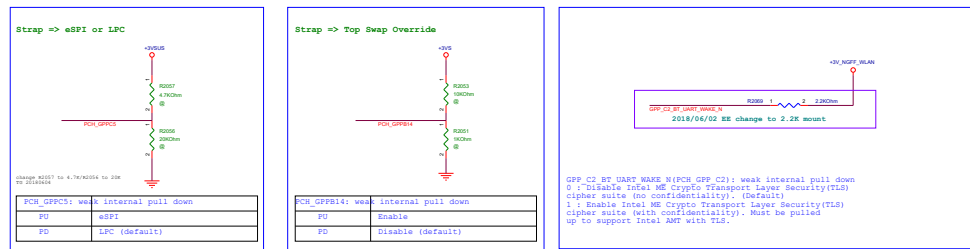
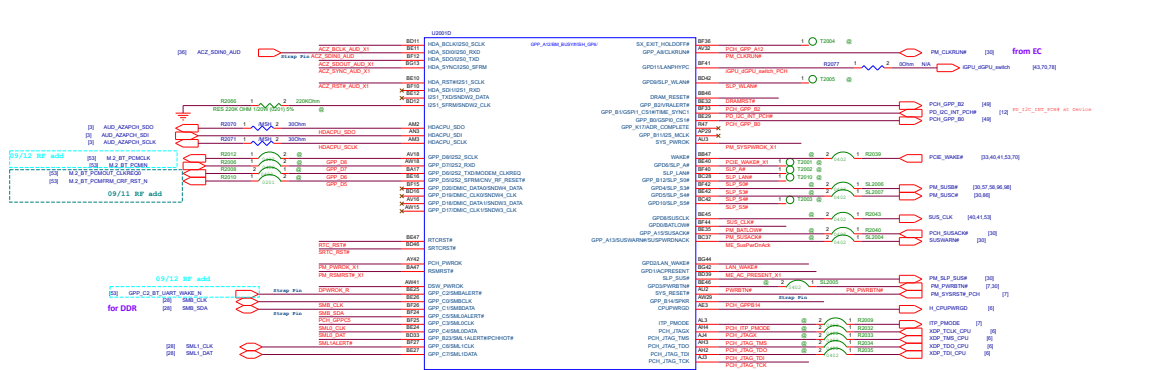
HD Audio



Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
	+1.05VSUS	+VCCST		
	+1.2V			
	+3VA0	+3VA	+3VA_EC	
	+3VSUS	+3VSUS_PCB		
	+3VA_DSW	+3VS		



USE RTC Battery:
 PIN: 06100-00040500 BATT-LI CR1220 3V



Only 3V Torlence

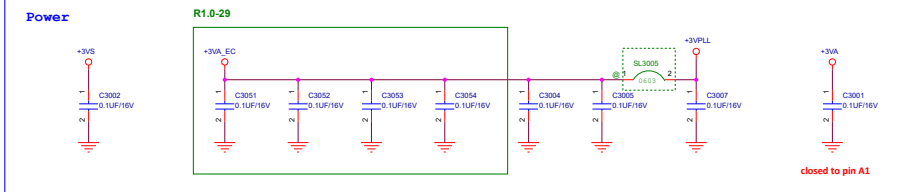
```
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI[0:7]
GPJ[0:7]
```

Can be adjusted to
Open-Drain for port:

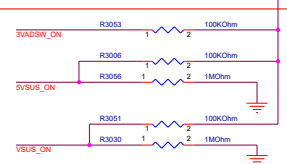
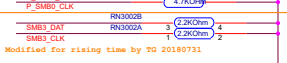
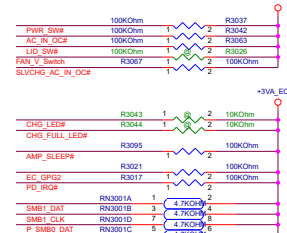
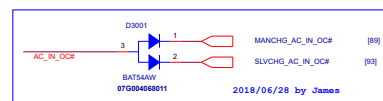
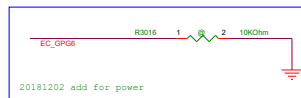
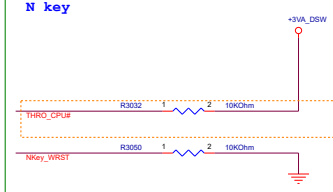
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

Power

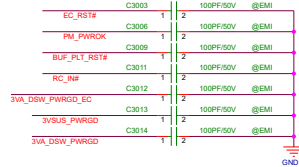


N key

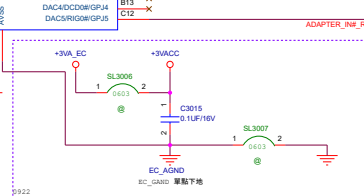
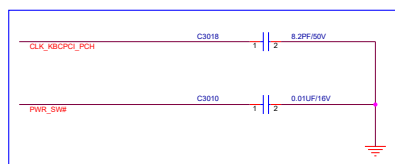
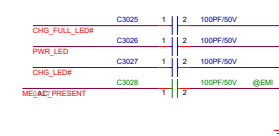


for load code

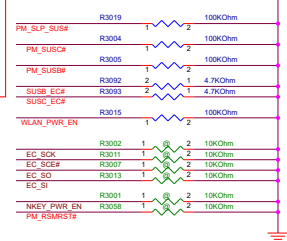
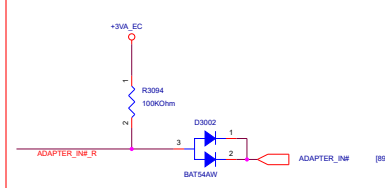
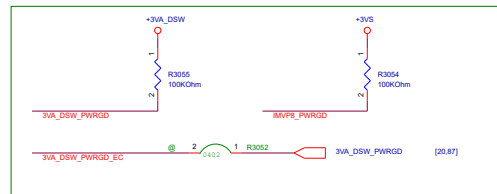
ITE Version	ASUS P/N
IT8225VG-128/CX	06037-00260300



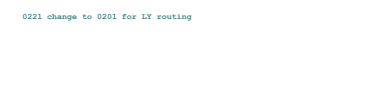
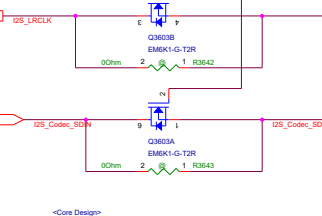
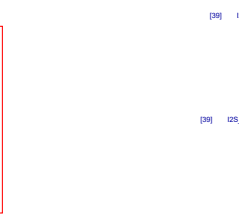
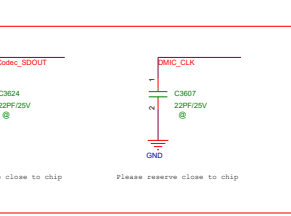
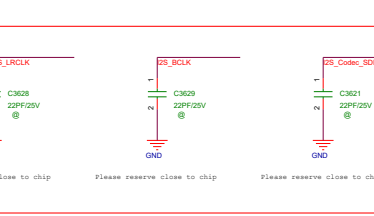
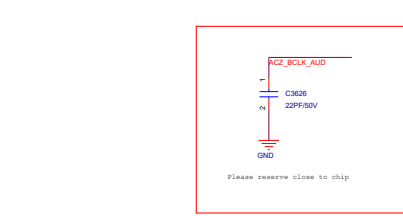
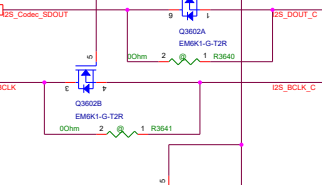
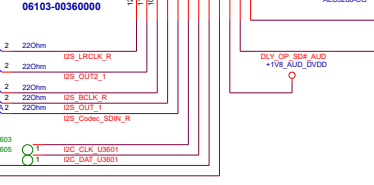
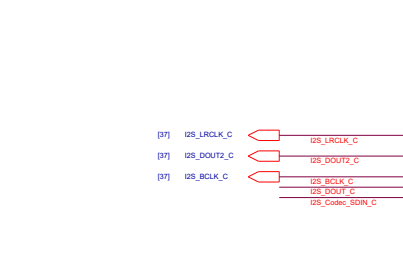
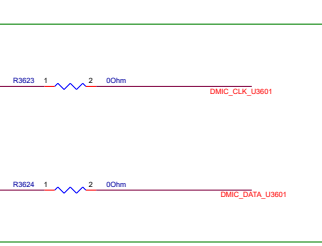
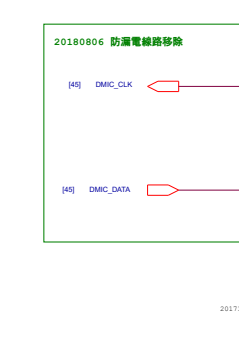
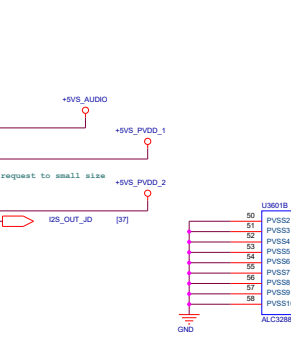
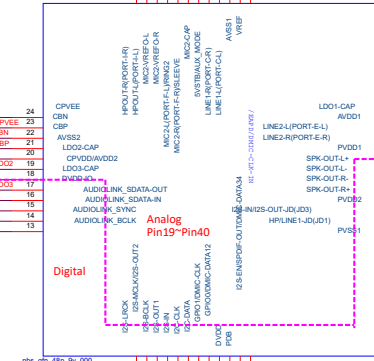
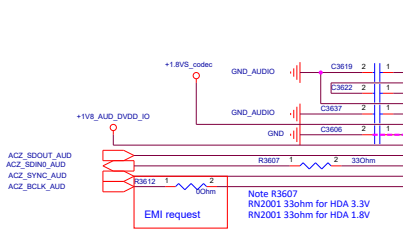
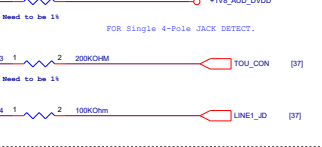
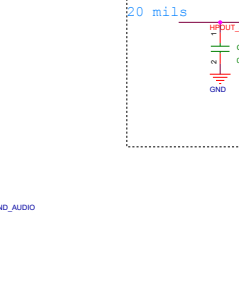
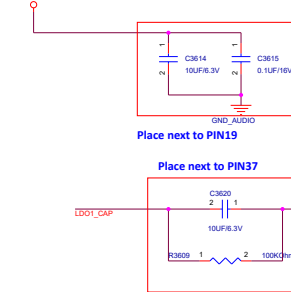
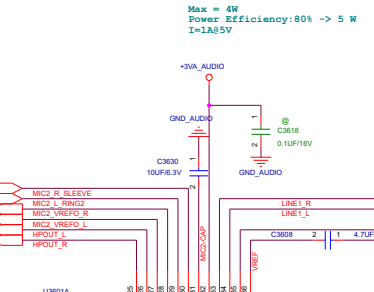
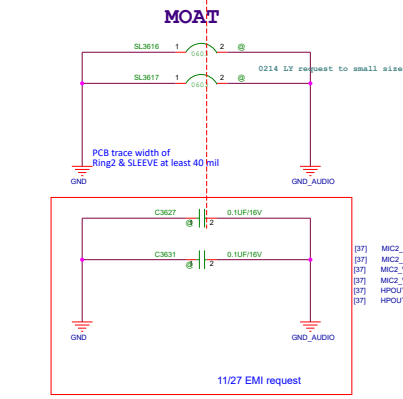
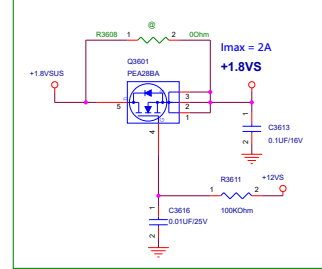
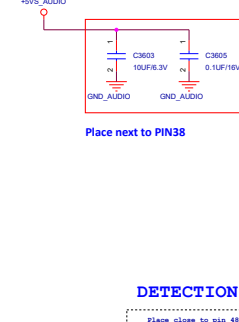
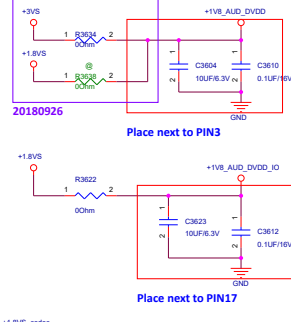
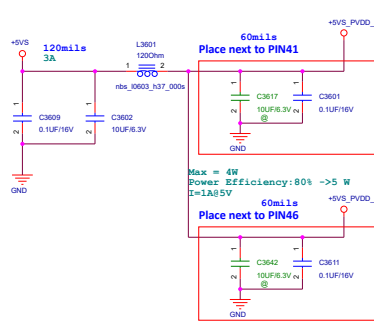
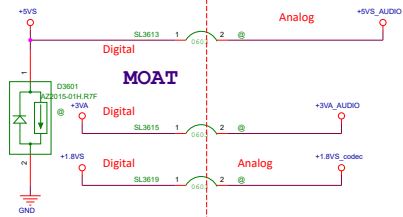
For EMI



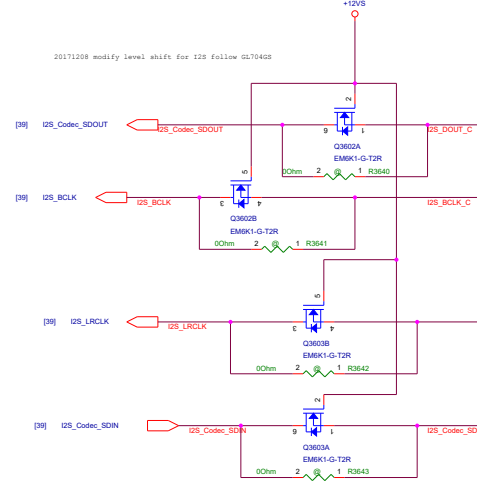
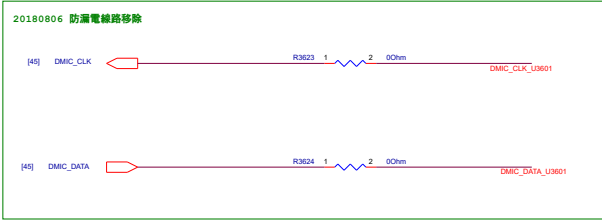
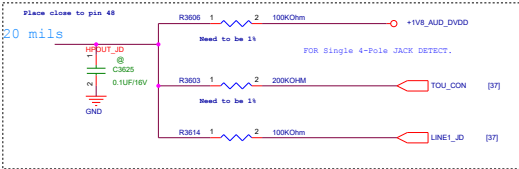
R1.0-34



<Core Design>



DETECTION

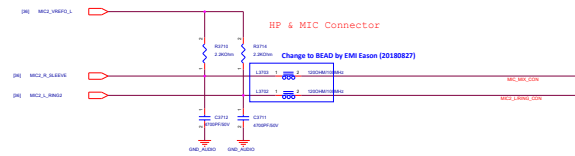
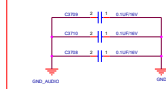


0221 change to 0201 for LY routing

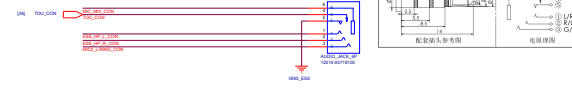
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Project Name		Rev
ASUS		R1.2
Title :		AUD ALC3288-CG
Size	Dept.:	ASUSTek COMPUTER INC. Engineer: EE
Date: Monday, February 18, 2019	Sheet	36 of 99

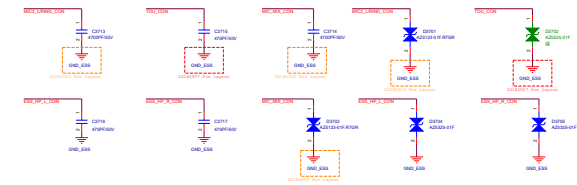
A_GND / GND



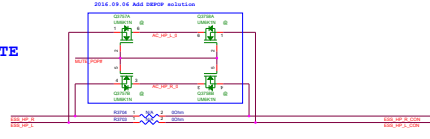
HP & MIC Connector



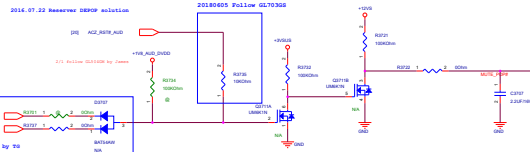
EMI



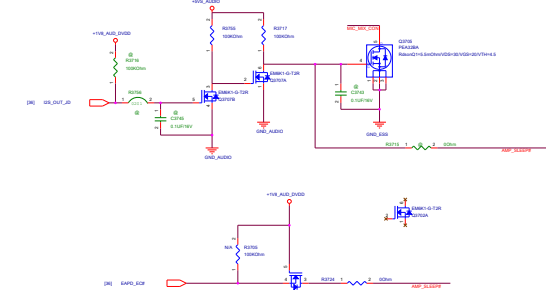
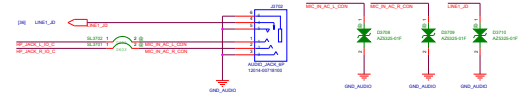
MUTE



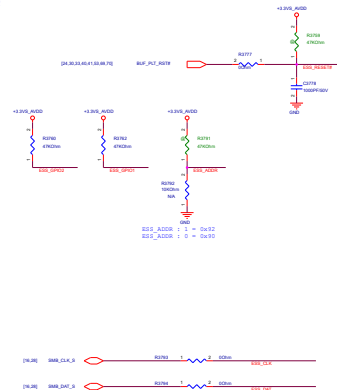
MUTE CONTROL



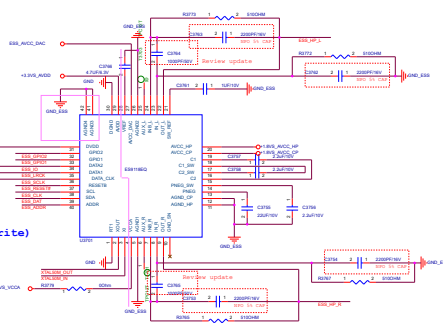
EXTERNAL MICROPHONE



ESS ES9118EQ

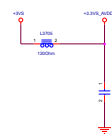


Address 0x90 (Write)

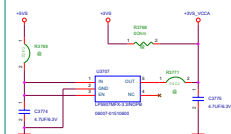


Modify 1216

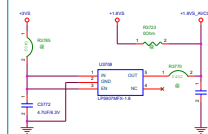
Codec LDO +3.3VS_AVDD



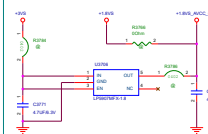
Codec LDO +3VS_VCCA



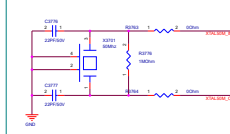
Codec LDO +1.8VS_AVCC_HP



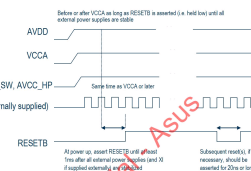
Codec LDO +1.8VS_AVCC_CP



50MHz XTAL

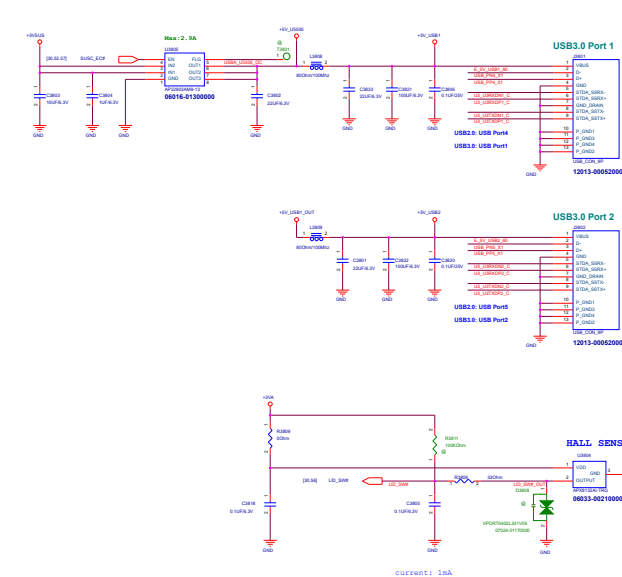


RECOMMENDED POWER UP SEQUENCE

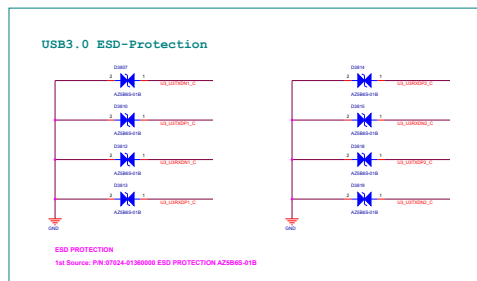
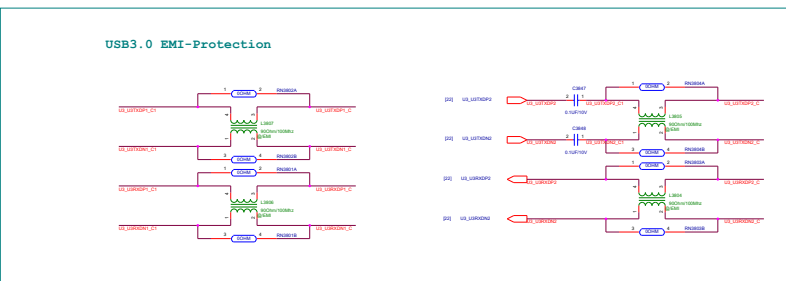
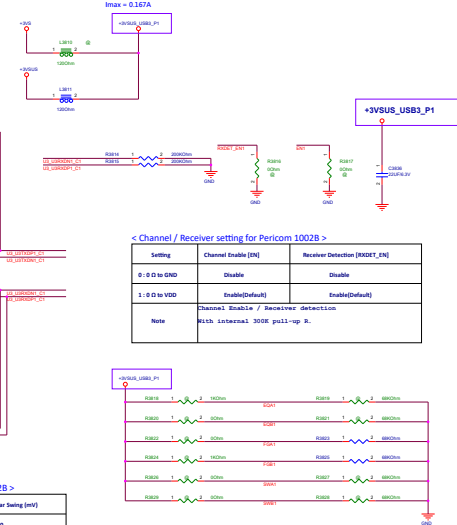
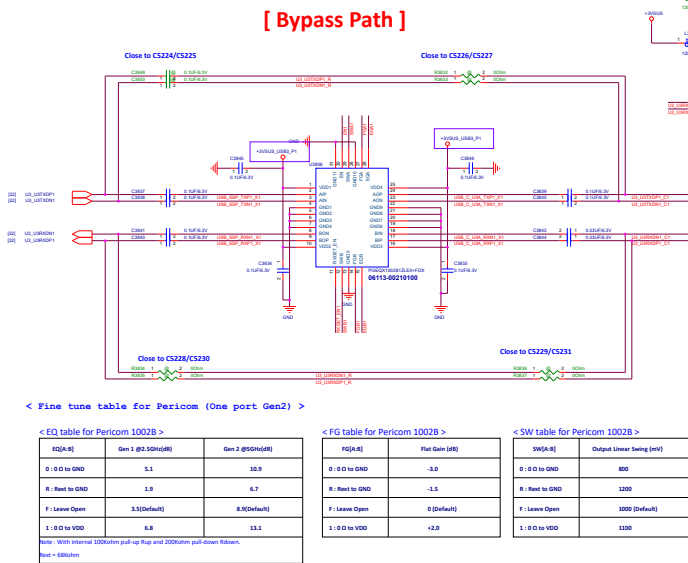


Driver 行為會follow 下表

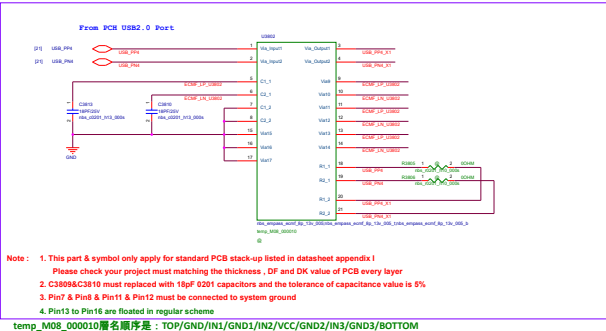
	EMIO_BCH	I2S_OUT_ID	MIC2_VREF0_R
Default	LOW	LOW	LOW
TTIA (I/A/R/M) Iphone	LOW	LOW	HIGH
DMTP (I/A/R/M/G) Nokia	LOW	HIGH	LOW
一般耳機	LOW	HIGH	HIGH
Speaker(揚音器)	HIGH	LOW	LOW
Speaker(不揚音器)	LOW	LOW	LOW



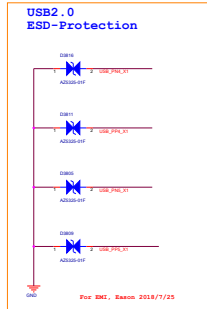
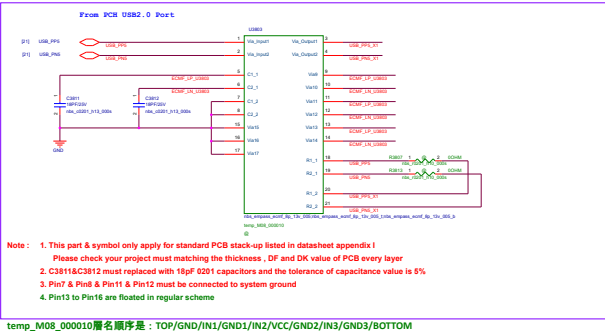
USB3.1_Port1 (Gen1)


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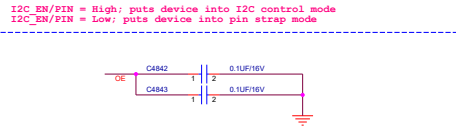
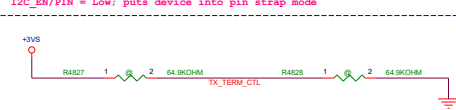
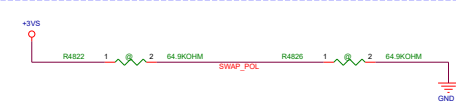
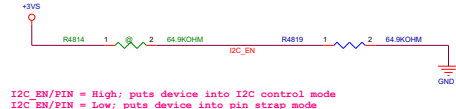
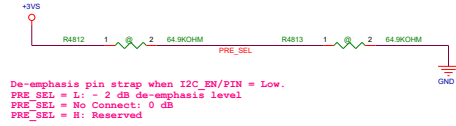
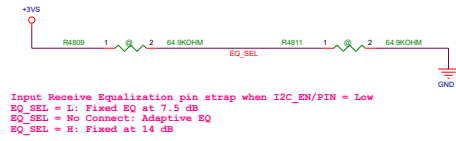
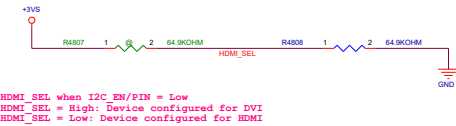
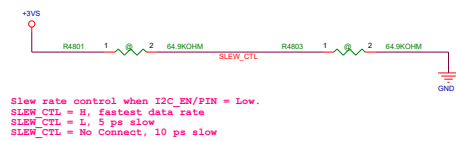
R1.6 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



R1.6 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

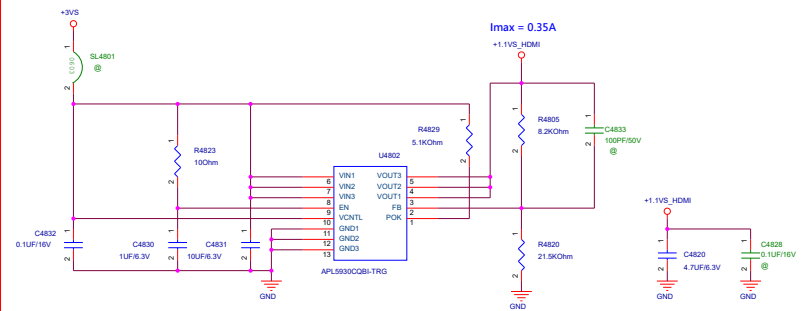


©Gee Design



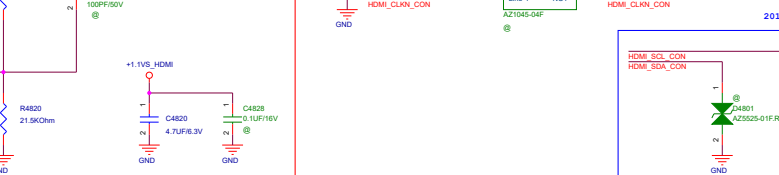
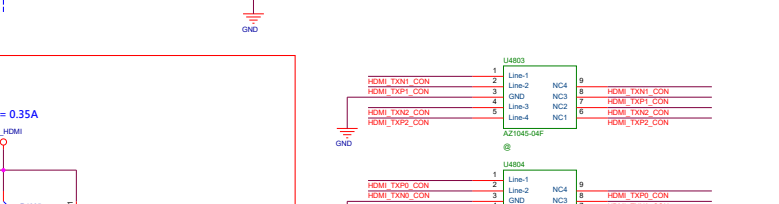
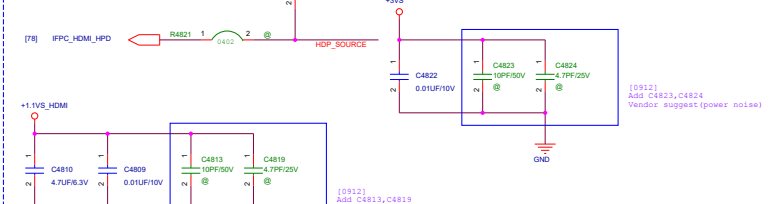
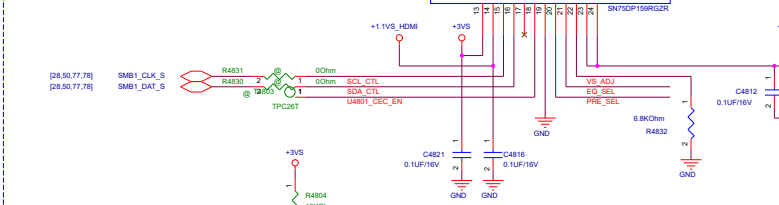
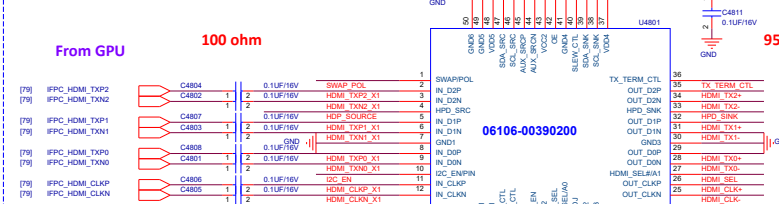
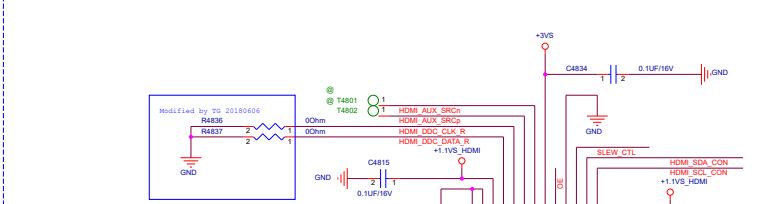
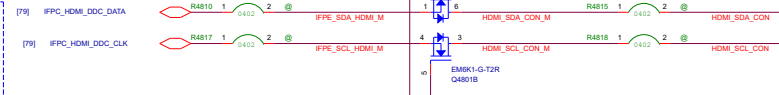
Operation enable/reset pin
 OE = L: Power-down mode OE = H: Normal operation
 Internal weak pullup: Resets device when transitions from H to L

HDMI LDO 1.1V5

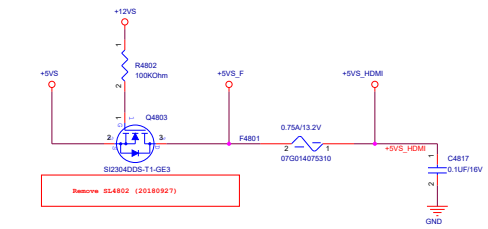


HDMI Active-Level Shift

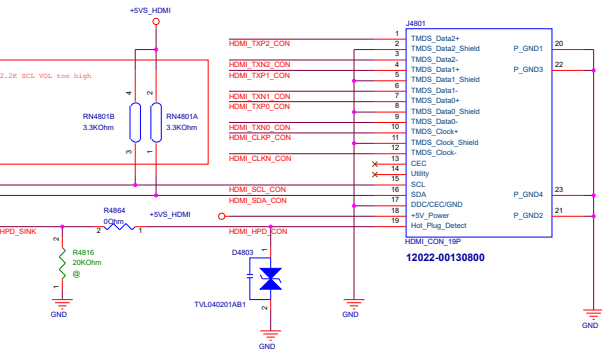
to GPU



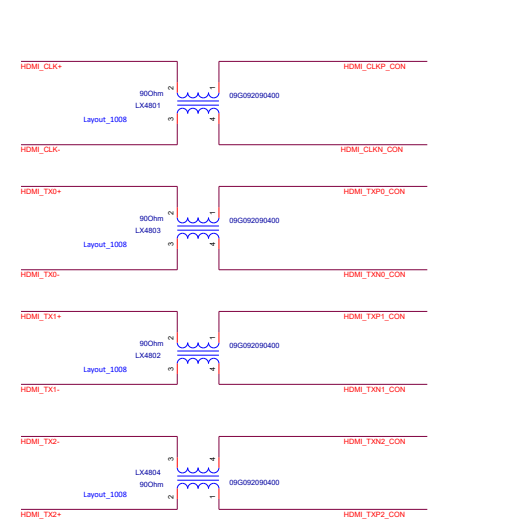
HDMI PWR_+5V5_HDMI



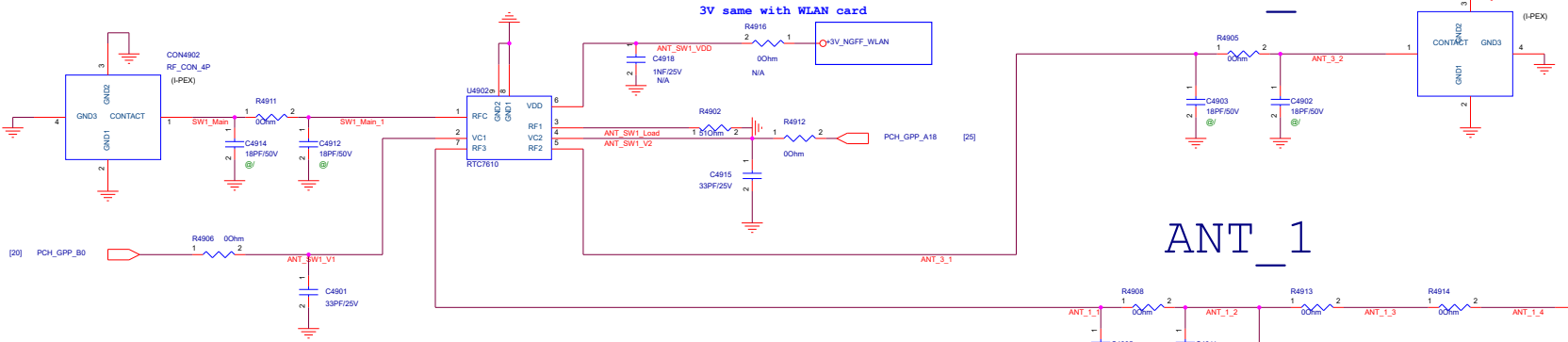
HDMI Conn.



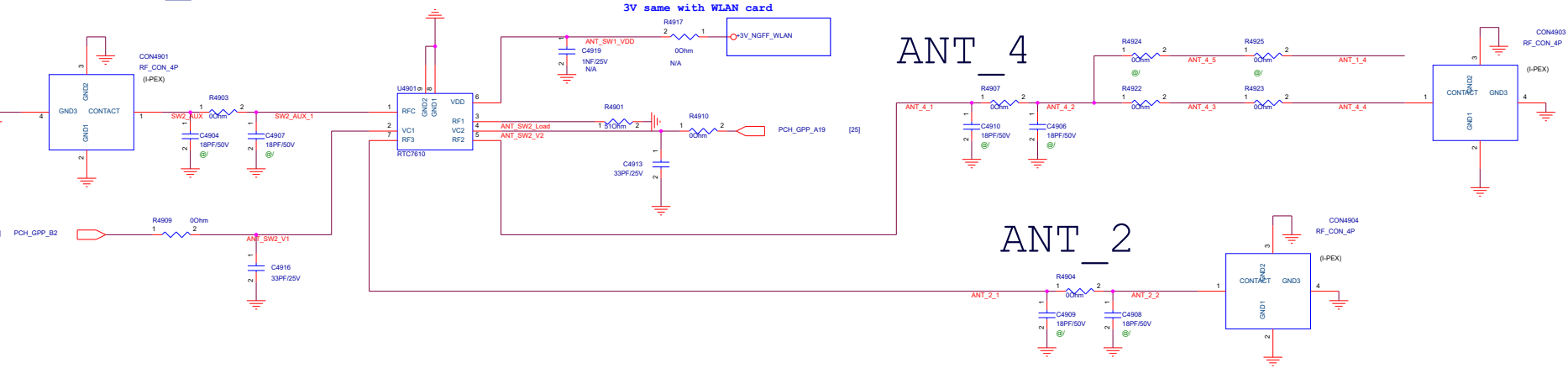
HDMI EMI



Module_Main



Module_AUX

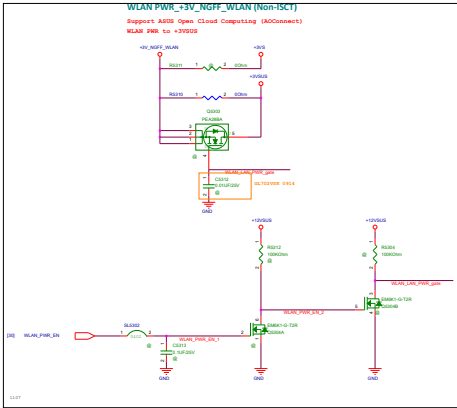
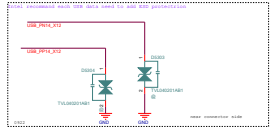
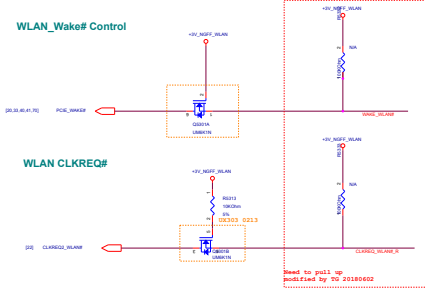
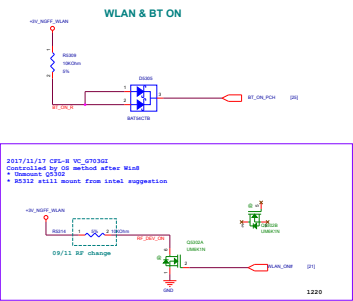


U4901 RTC7610				
AUX	Port	V1	V2	V3
ANT_4	RF1	GPP_B2	GPP_A19	
ANT_2	RF2			
50 Ω	RF3			

U4902 RTC7610				
Main	Port	V1	V2	V3
ANT_3	RF1	GPP_B0	GPP_A18	
ANT_1	RF2			
50 Ω	RF3			

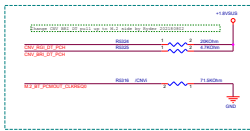
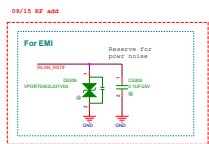
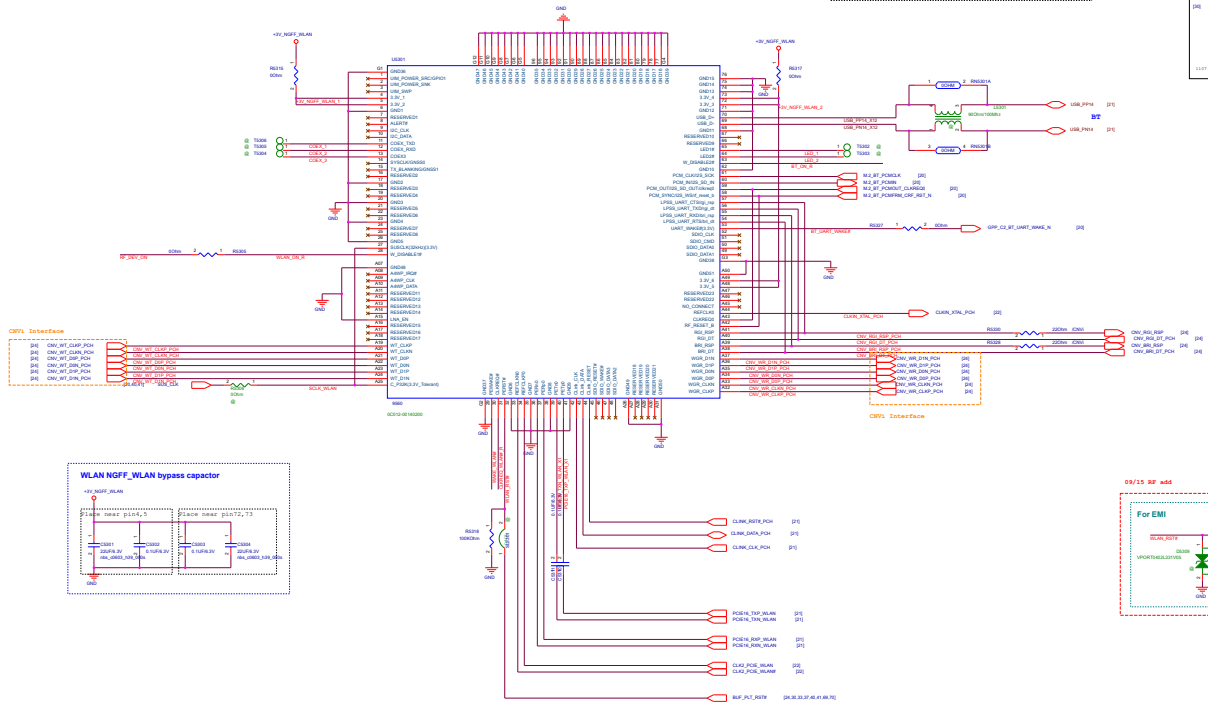
0: 0 v ~ 0.3v
1: 3 v ~ 3.6v

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2017.03.15 Connector list update

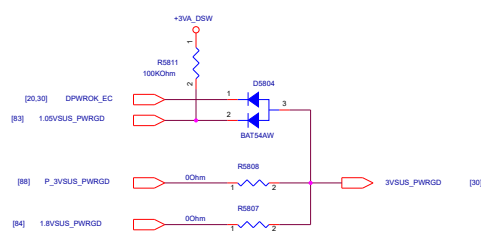
SD-1216



Cloud Design

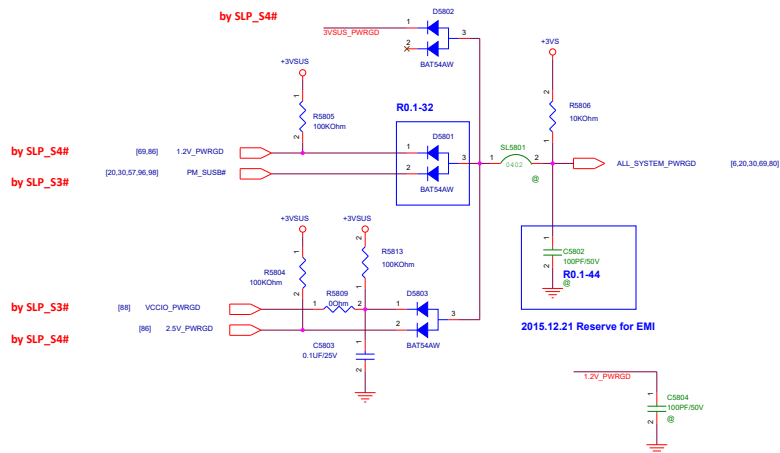
SUS_VR_PWRGD [

SLP_SUS_N
V0.85_PWRGD
V3.3A_VSA_PWRGD
V1.0A_PWRGD
V1.8A_PWRGD
DPPWRK=3.3A_DSHPWRGD+10ms & BATT>5.35V



[ALL_SYSTEM_PWRGD]

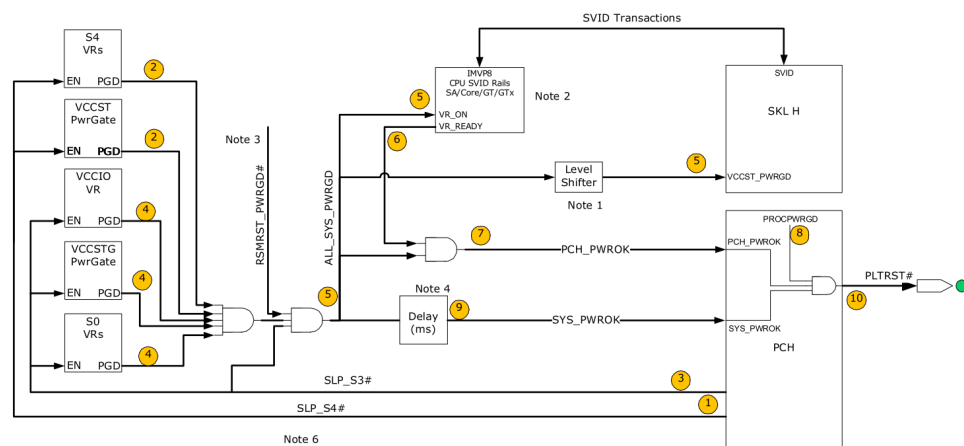
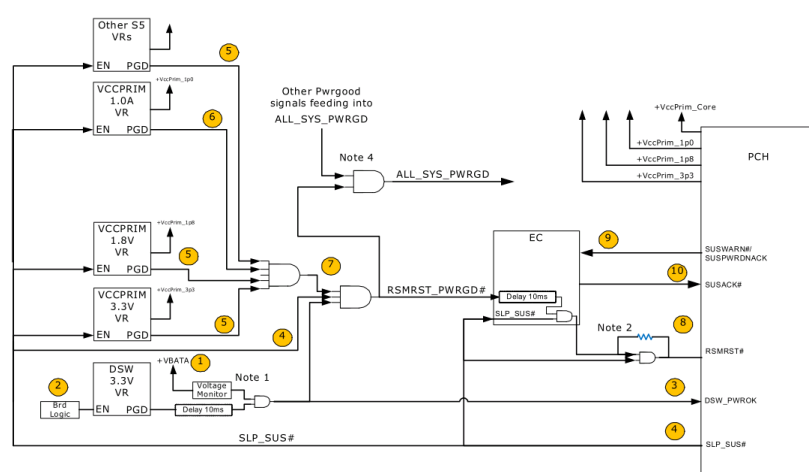
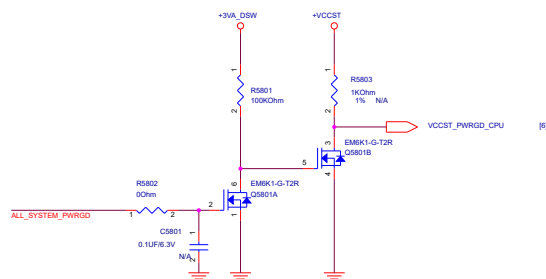
SLP_S3_N
DDR_PWRGD
VCCIO_PWRGD
3.3S_MON
1.00U_MON
1.8S_MON
RSMRST_PWRGD
SYS_PWROK



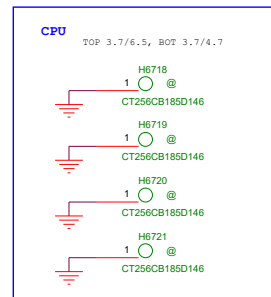
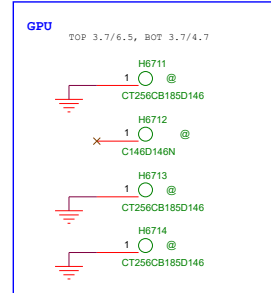
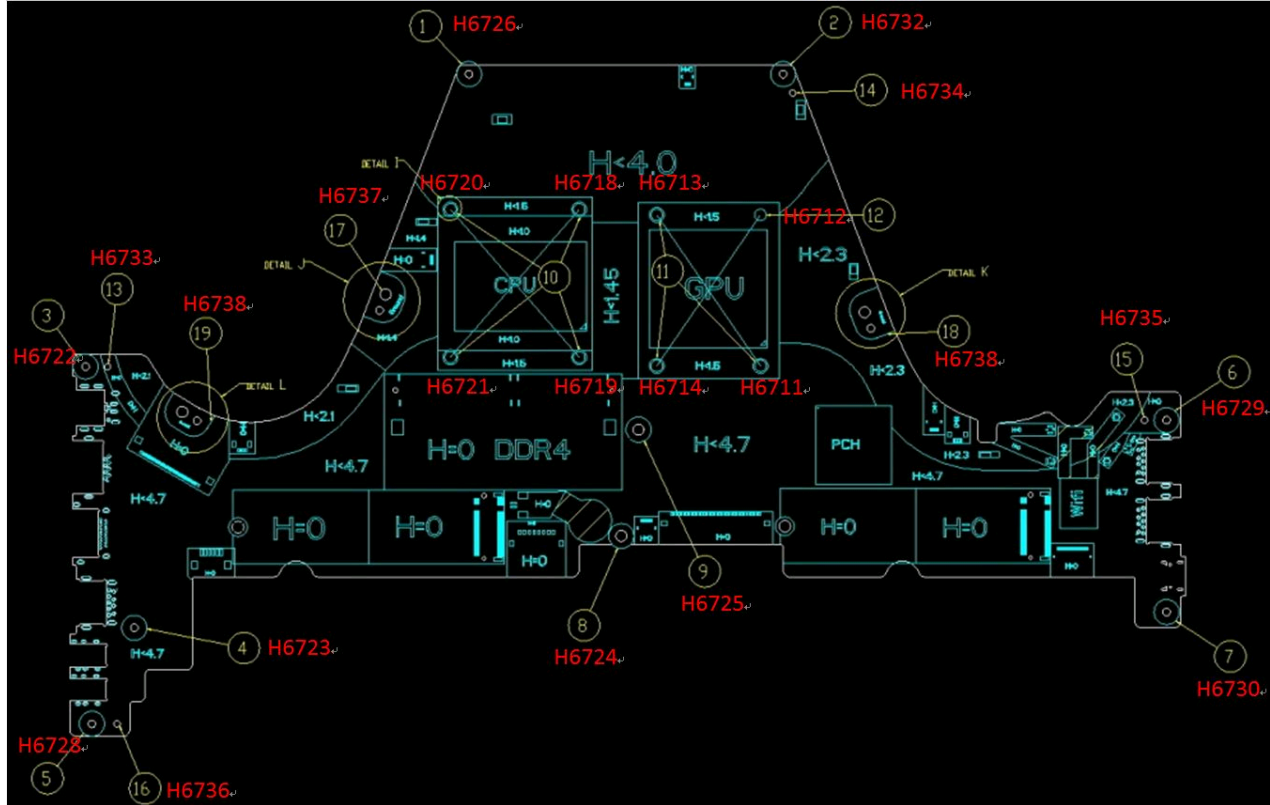
by SLP_S4#
by SLP_S3#

by SLP_S3#
by SLP_S4#

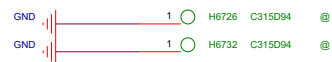
[VCCST_PWRGD for PCH]



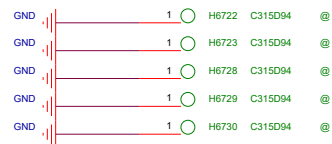
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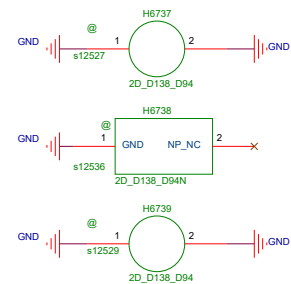
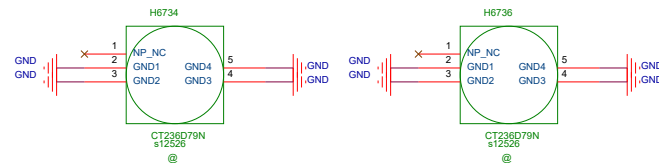
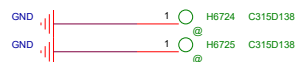
TOP&BOT 2.4/8



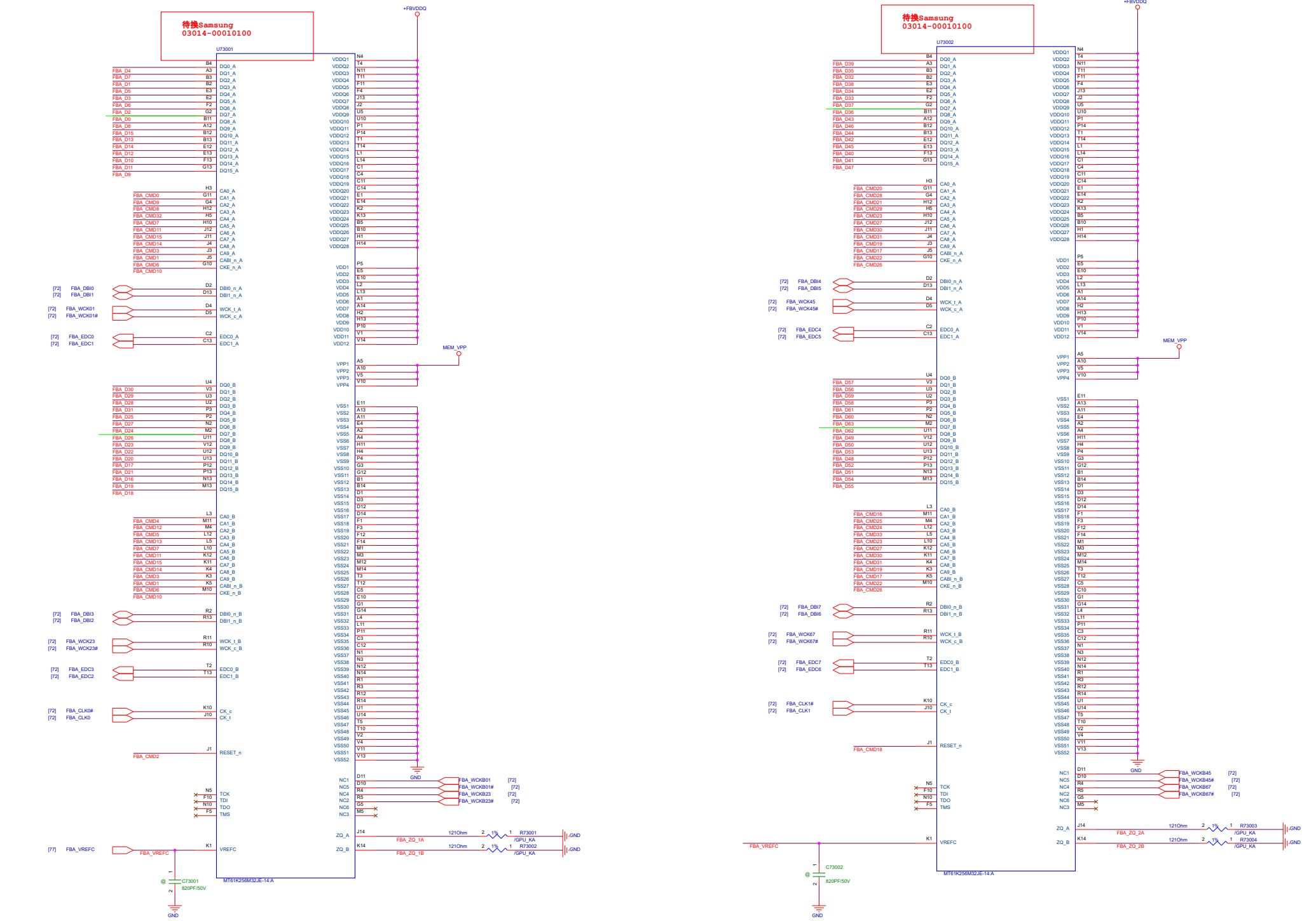
不裸銅NPTH




TOP&BOT 3.5/8

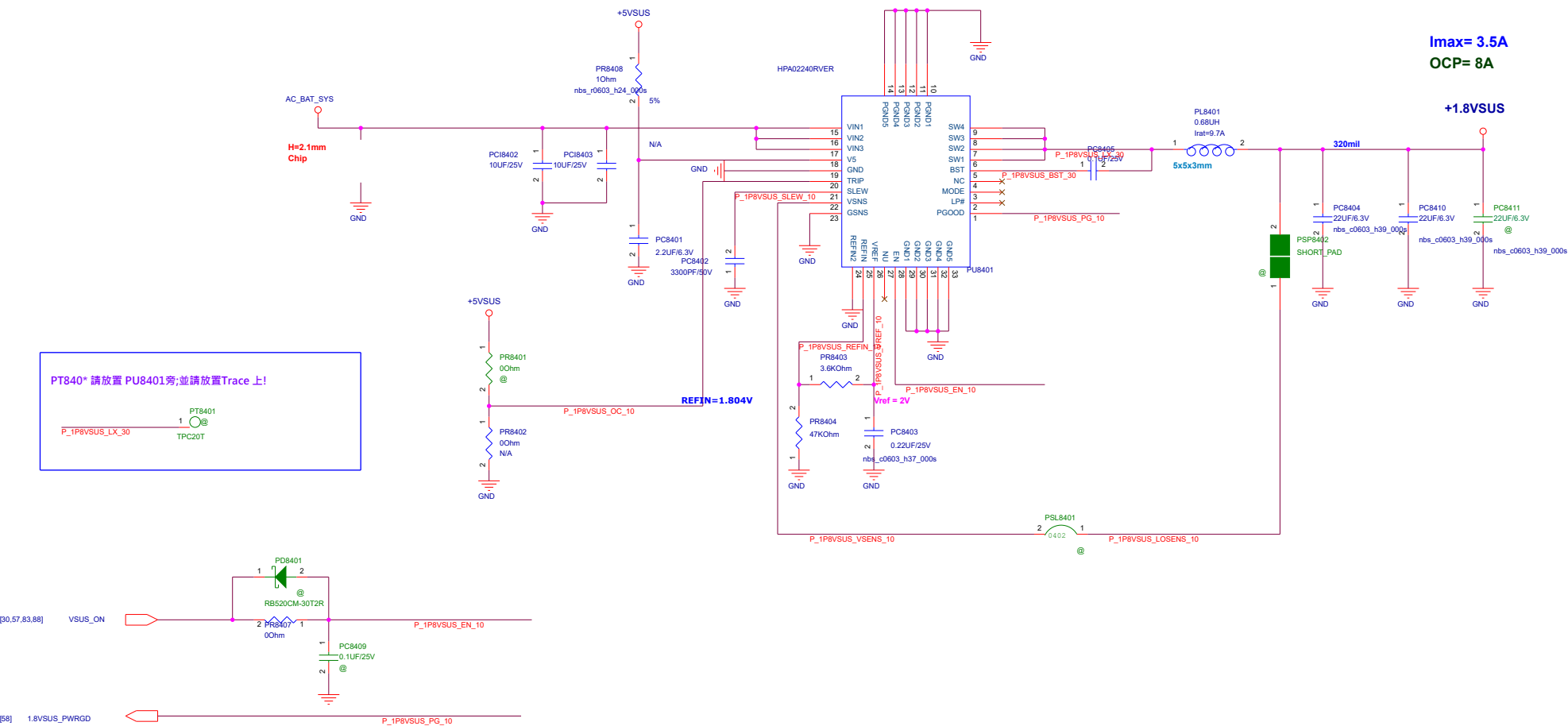



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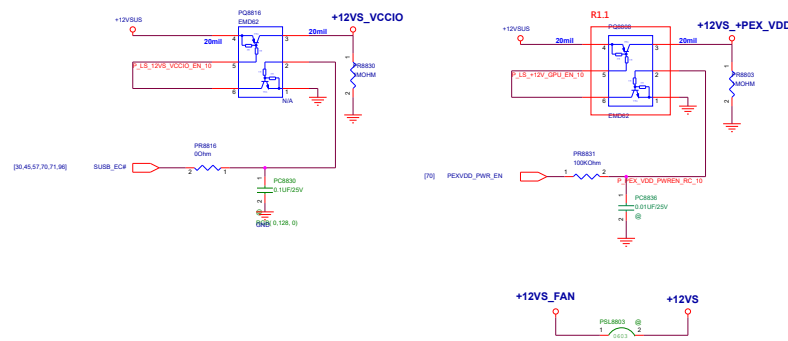
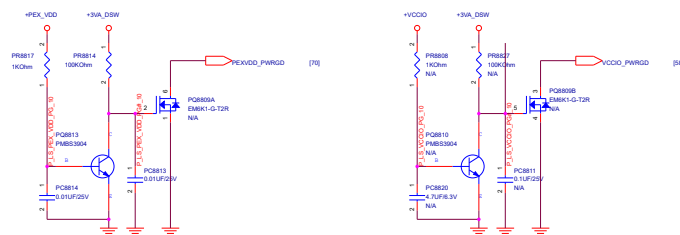
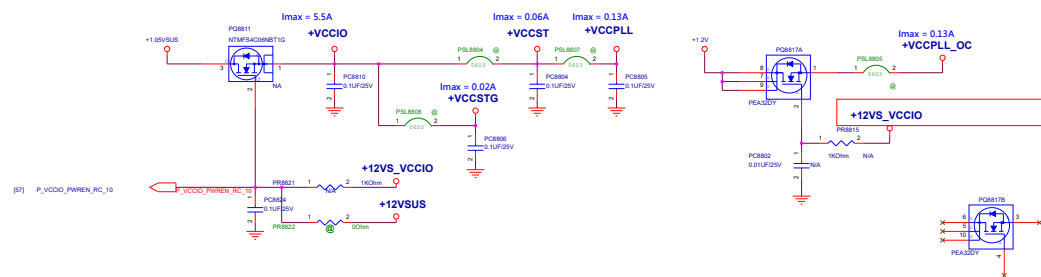
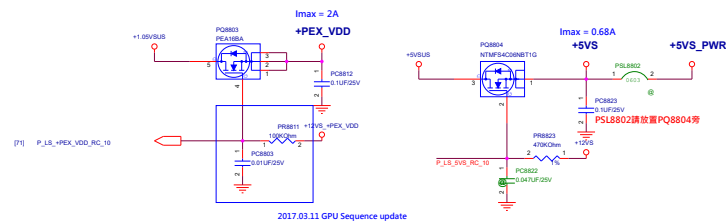
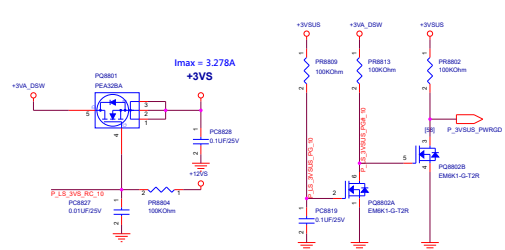
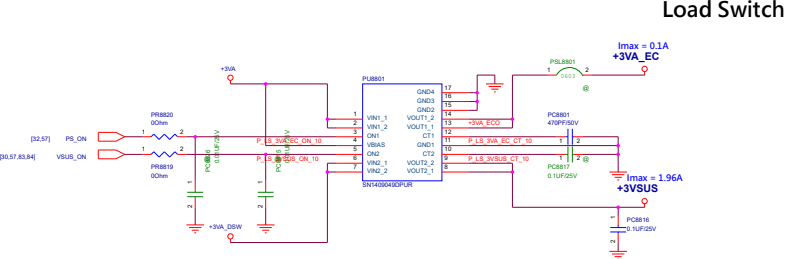


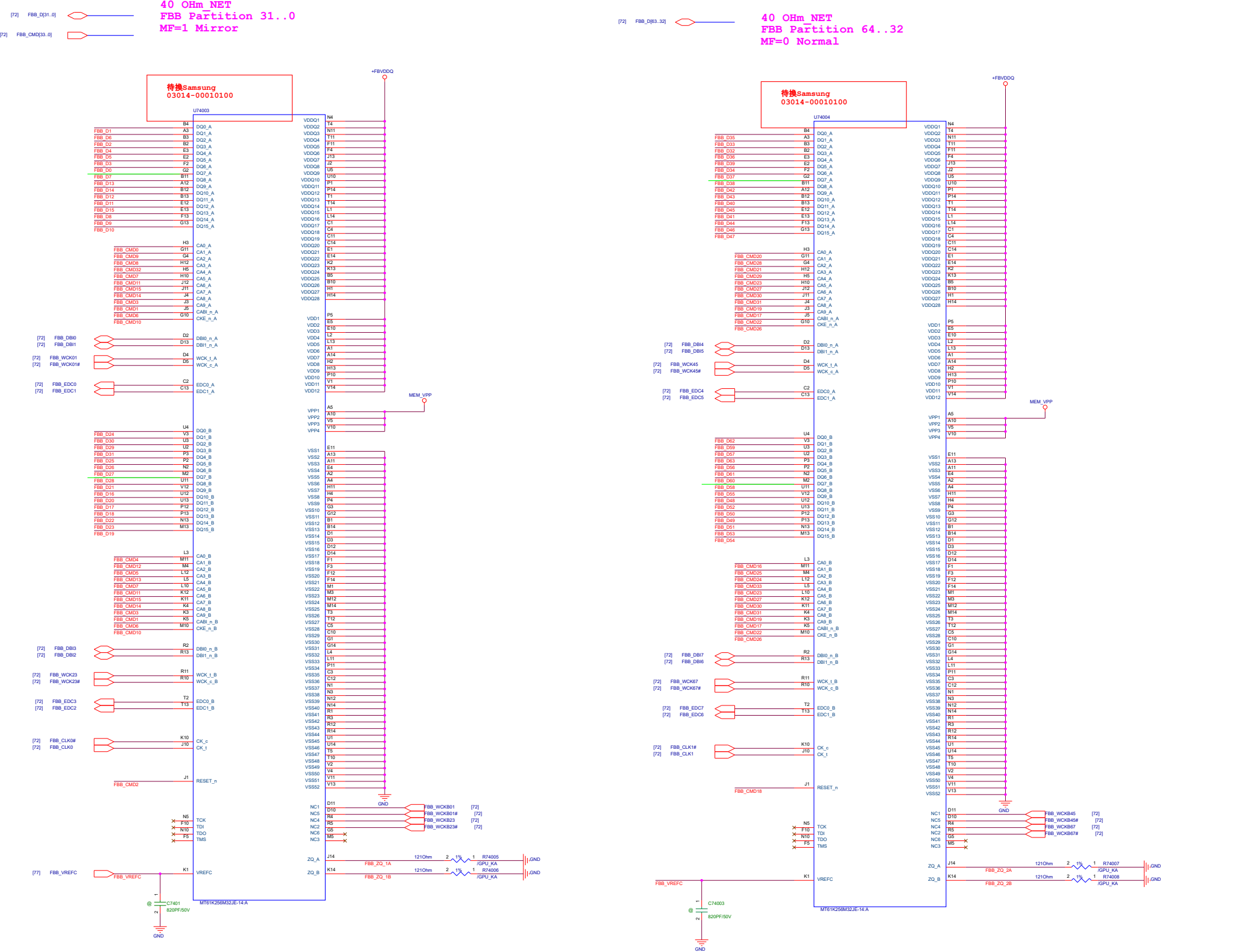
		Title : OTH_for test only	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 82 of 99	


+1.8VSUS [For PCH]



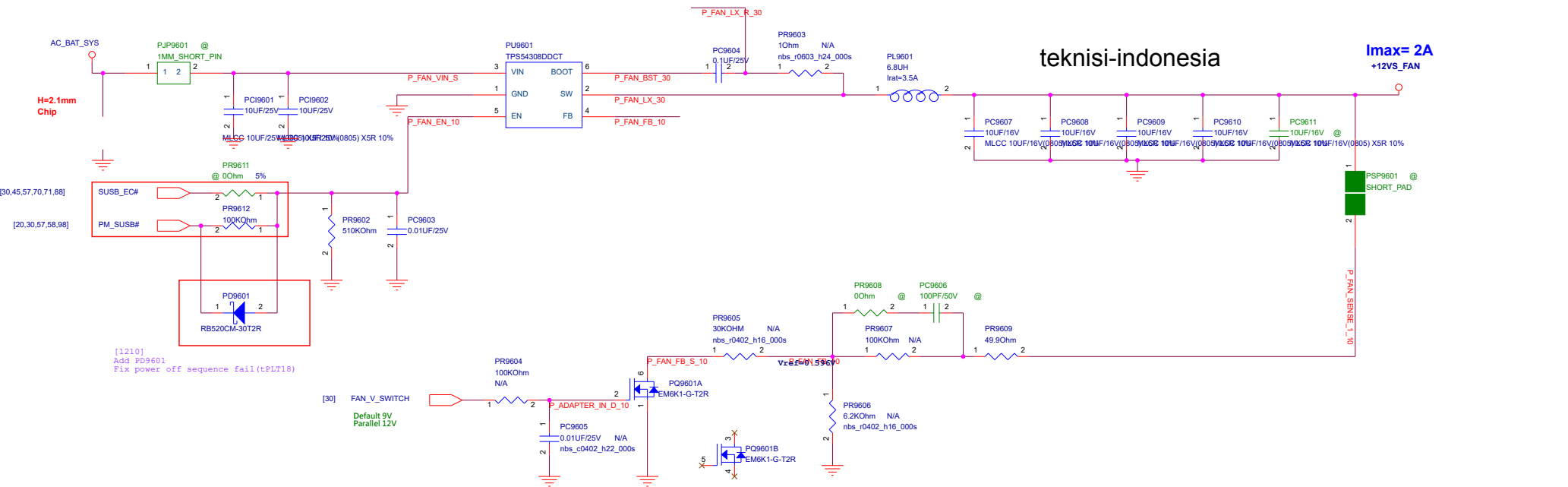
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ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 85 of 99	






		Title : OTH_for test only	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 95 of 99	

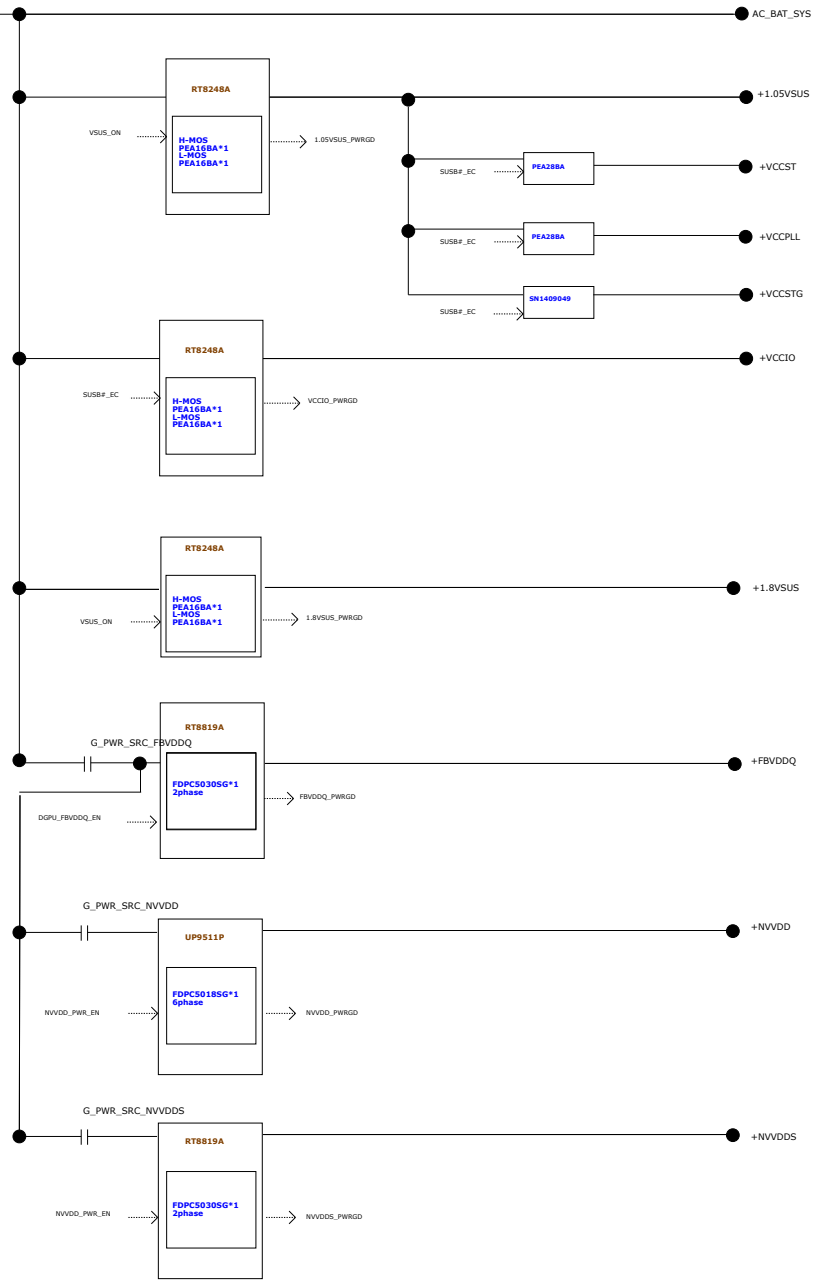
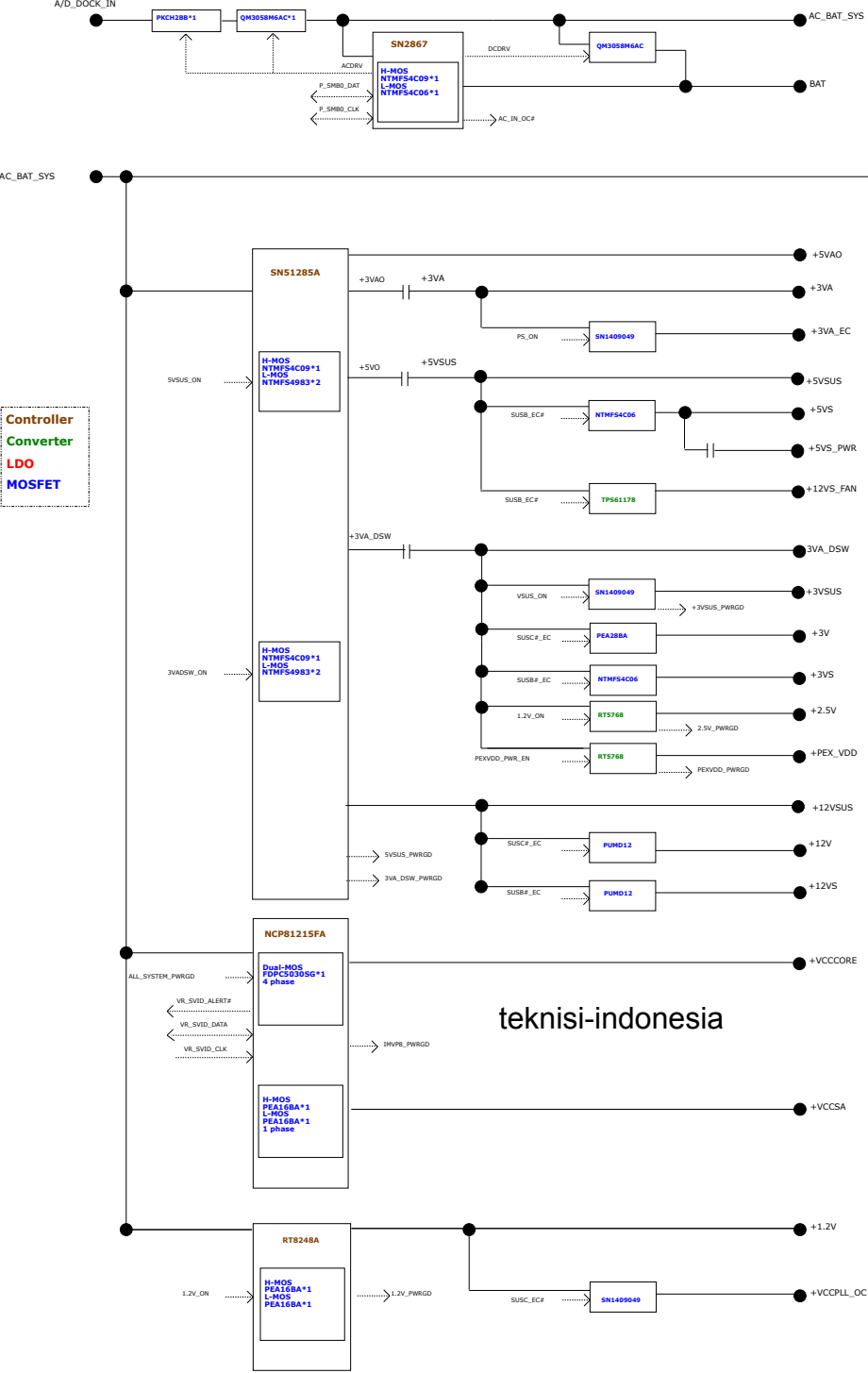
+12VS_FAN [For FAN]



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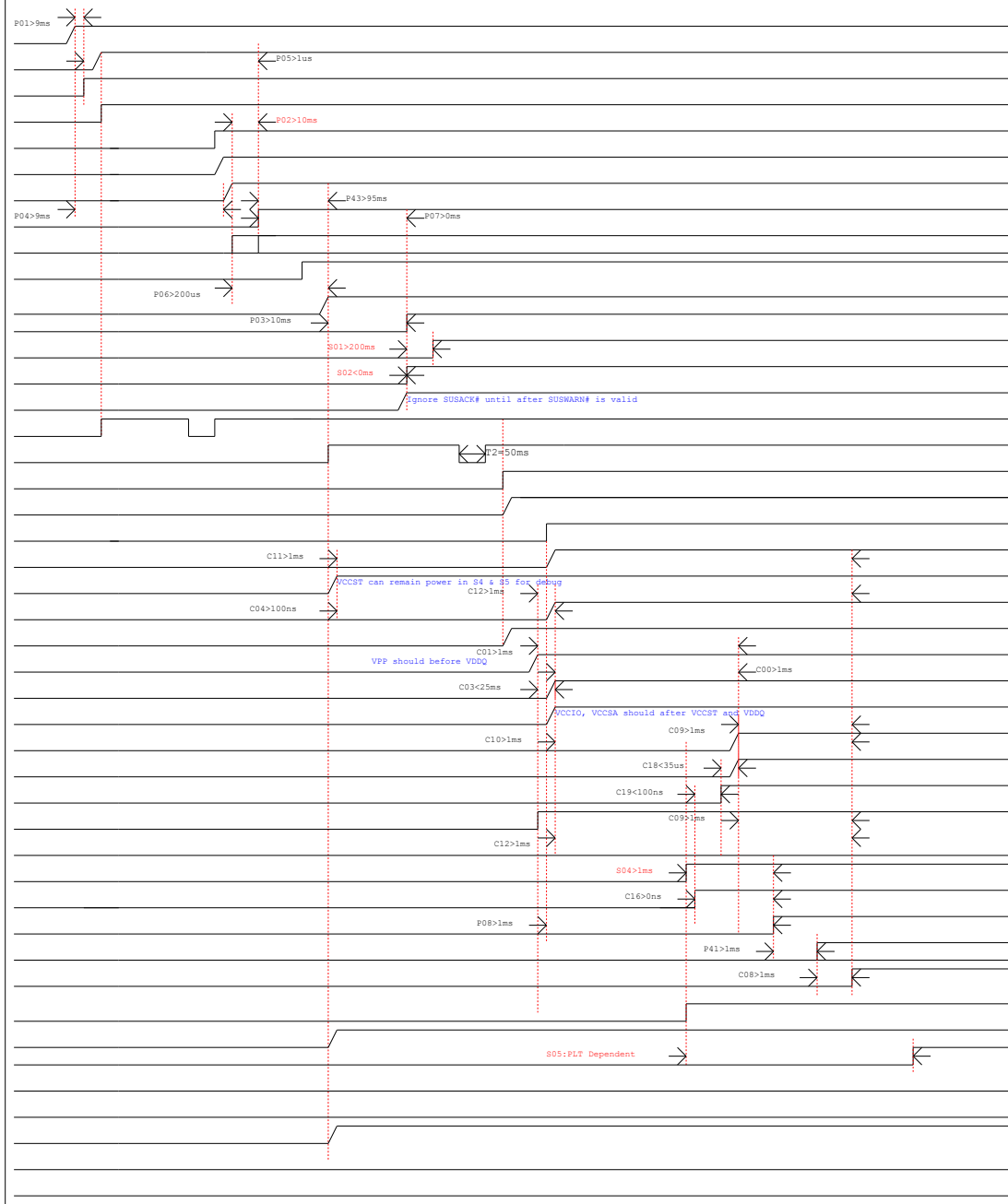
ASUS		Project Name	Rev
GX502GX			R1.2
Title : PW_+12VS_FAN			
Size	Dept.:	Engineer:	
B	NB Power team	Hon	
Date: Monday, February 18, 2019	Sheet	96	of 99

		Title : OTH_for test only	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Monday, February 18, 2019		Sheet 97 of 99	



DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
 P:PCH (AC_BAT_SYS)+3VA/+5VA
 S:PLT (+3VA_RTC) RTCRST# (PCH)
 Power (Power) AC_IN_OC# (EC)
 Signal (EC) PS_ON (+3VA_EC)
 (PS_ON)+3VA_EC (EC)
 (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
 (EC) DPWROK_EC (PCH)
 (+3VA_DSW) PM_BATLOW# (PCH)
 (PCH) PM_SLP_SUS# (EC)
 (VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
 (EC) PM_RSMRST#_PCH (PCH)
 (PCH) SUSWARN# (EC)
 (EC) ME_AC_PRESENT_PCH (PCH)
 (EC) PCH_SUSACK# (PCH)
 (PWR_Switch) PWR_SW# (EC)
 (EC) PM_PWRBTN# (PCH)
 (EC) SUSC_EC# (Power)
 (SUSC_EC#)+12V/+5V/+3V
 (EC) SUSB_EC# (Power)
 (SUSB_EC#)+12VS/+5VS/+3VS
 (VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
 (+VCCIO)+VCCSTG
 (1.2V_ON)+2.5V (2.5V_PWRGD)
 (1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
 (+12VS)+VCCPLL_OC
 (SUSB_EC#)+VCCIO (VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU) DDR_VTT_CTRL (Power)
 (Power) 1.2V_PWRGD (AND)
 (Power) IMVP8_PWRGD
 (AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
 (EC) PM_PWROK_PCH (PCH)
 (PCH) CLK_PCH_BCLK (CPU)
 (PCH) H_CPU_PWRGD (CPU)
 (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
 (CPU) P_SVID_DATA_X2 (Power)
 (EC) PM_SYSPWROK_PCH (PCH)
 (PCH) PLT_RST# (CPU/EC/Device)
 (P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
 (CPU) H_THERMTRIP# (PCH)
 (PCH) DDR4_DRAMRST# (Memory)
 +VCCGT



CFL H Power Sequence (DC mode)

Rev	Date	Description

Rev	Date	Description

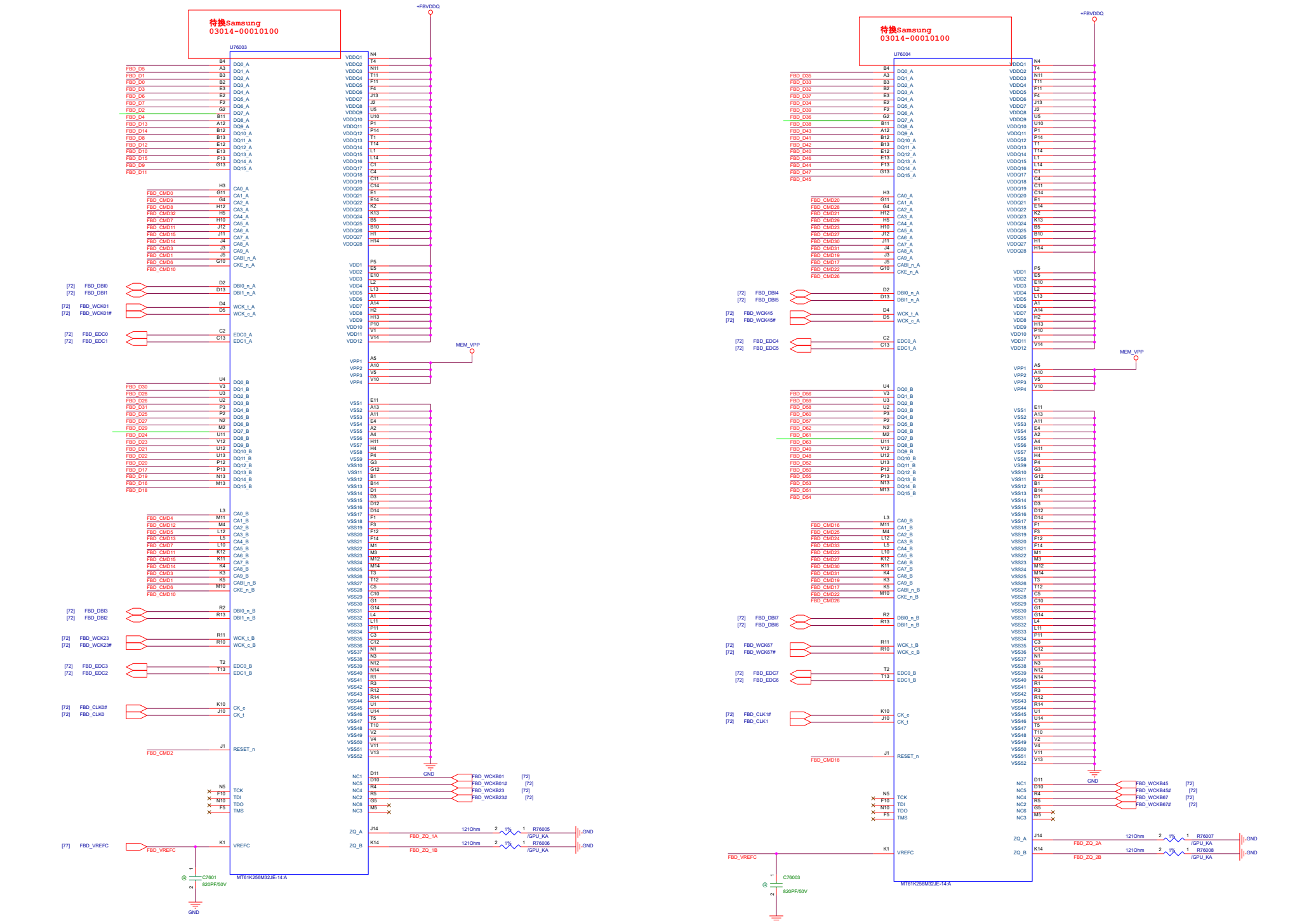
	Rev	Date	Description	Rev

[illegible]

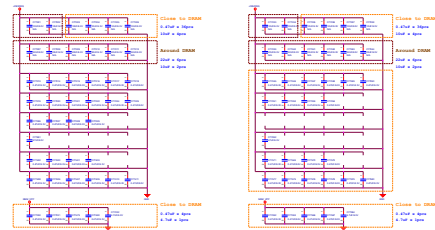
GX502GX R1.1 SKU Table

Option	PCB	SKU	CPU	Power	DIMM	VRAM			

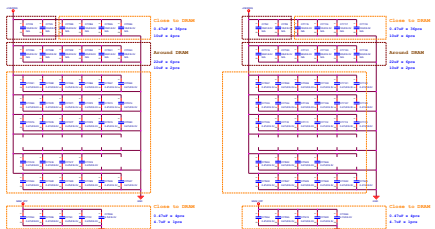
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Product Name: COMPUTER		Engineer: EE	
Part No. : GX502GX			
Rev. : 1.1			



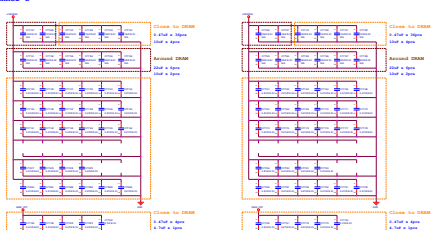
Channel A



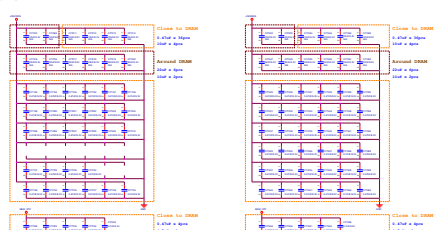
Channel B



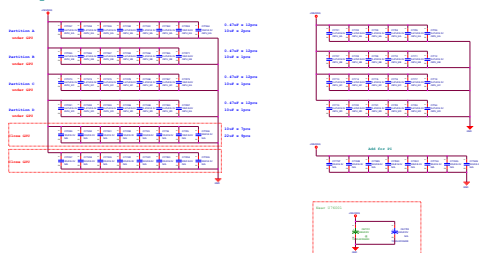
Channel C



Channel D



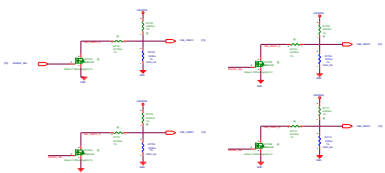
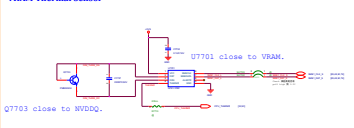
VRAM FVDDQQ

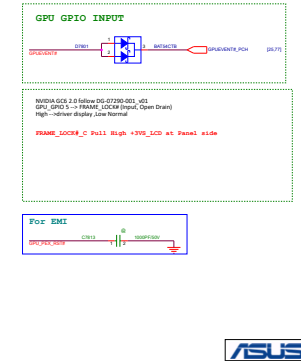
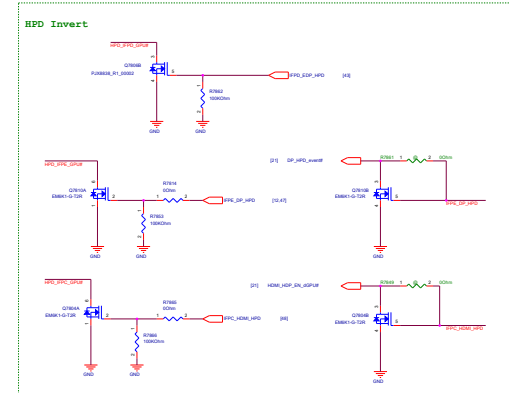
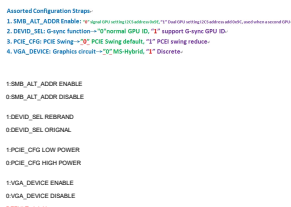
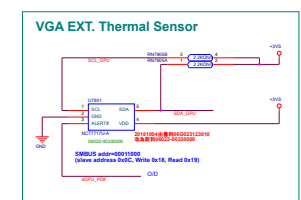
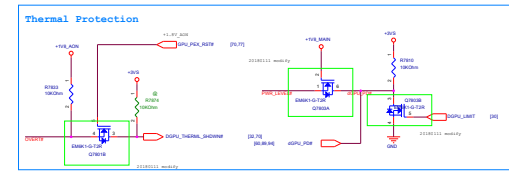
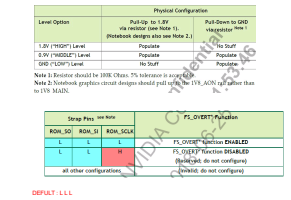
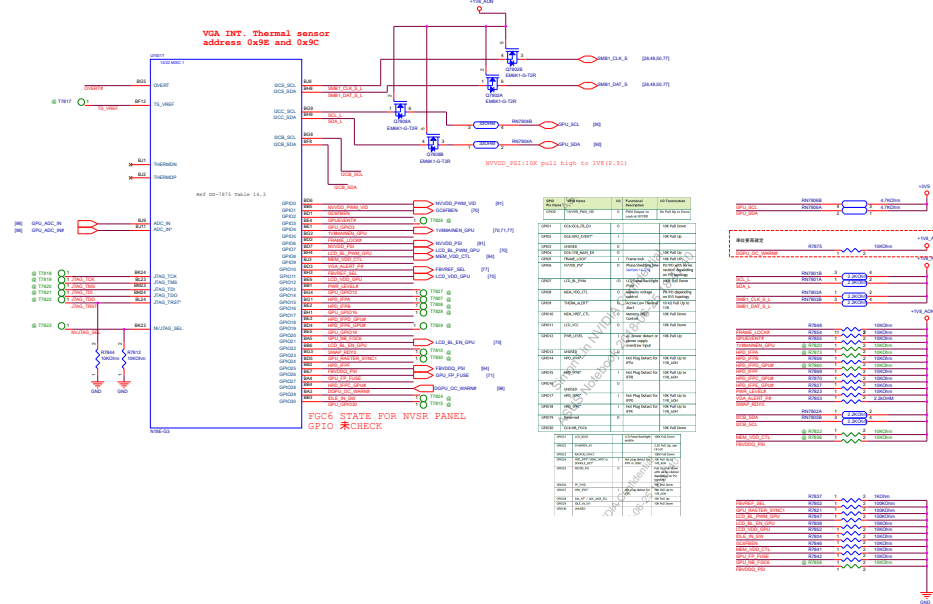


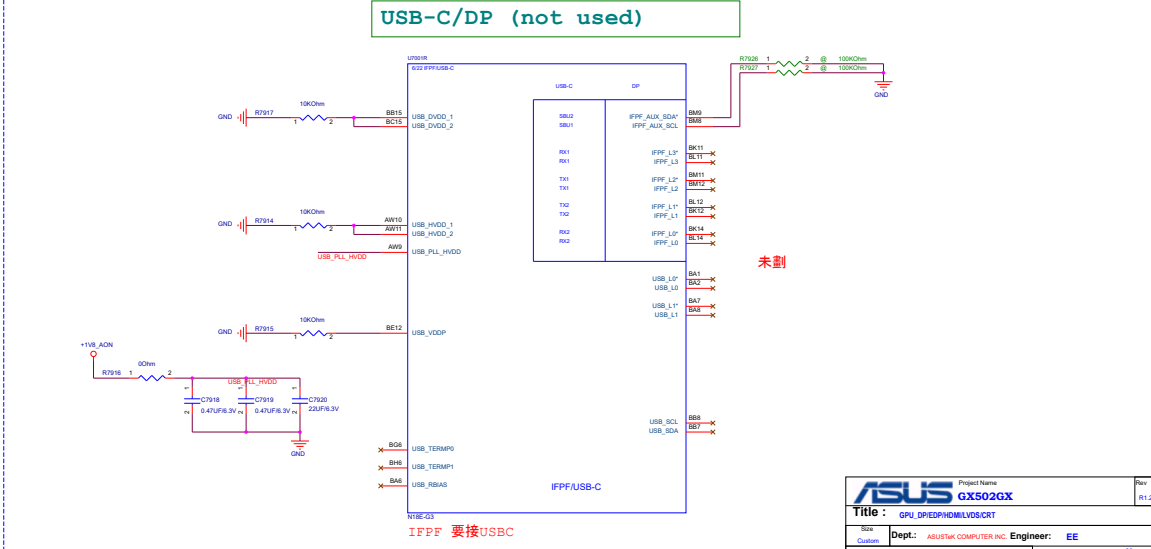
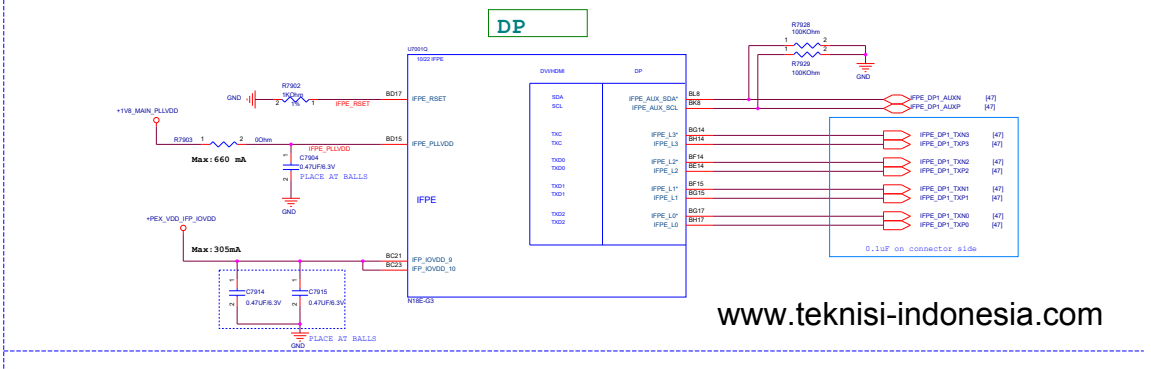
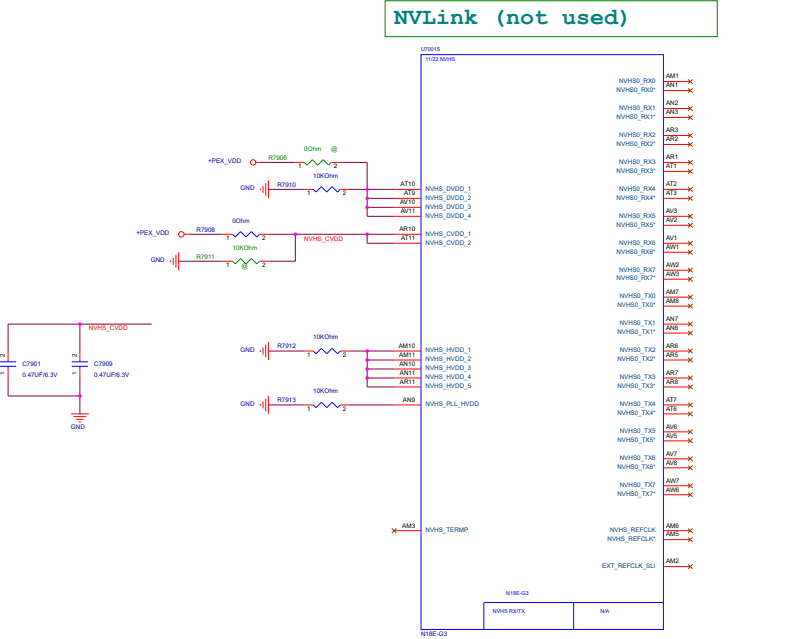
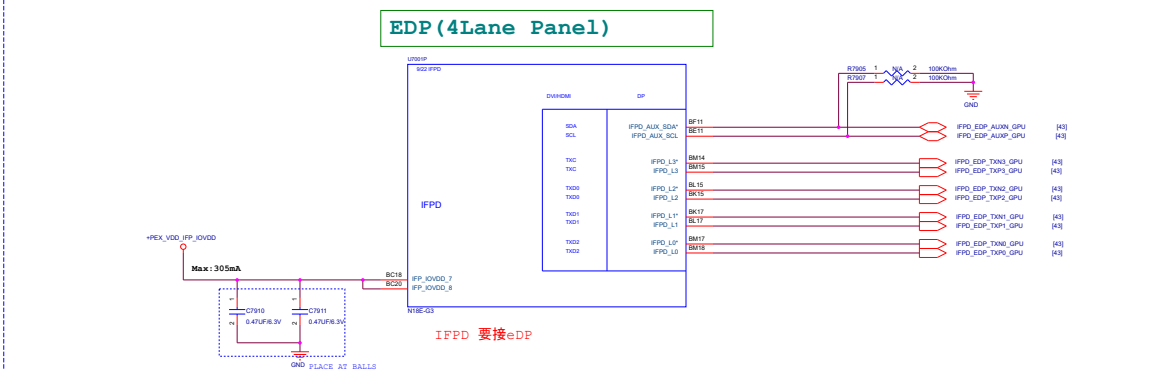
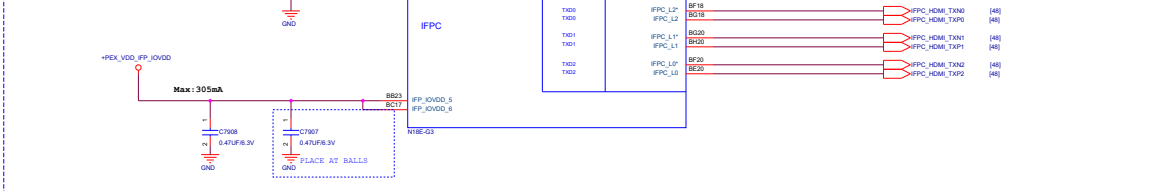
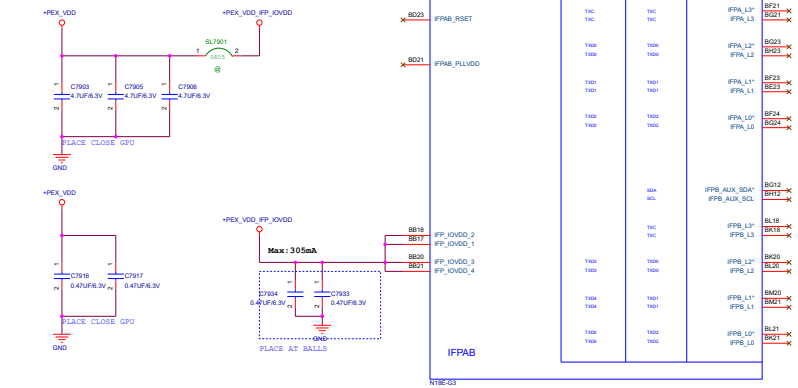
For power response measurement



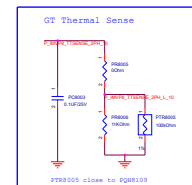
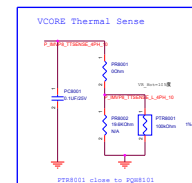
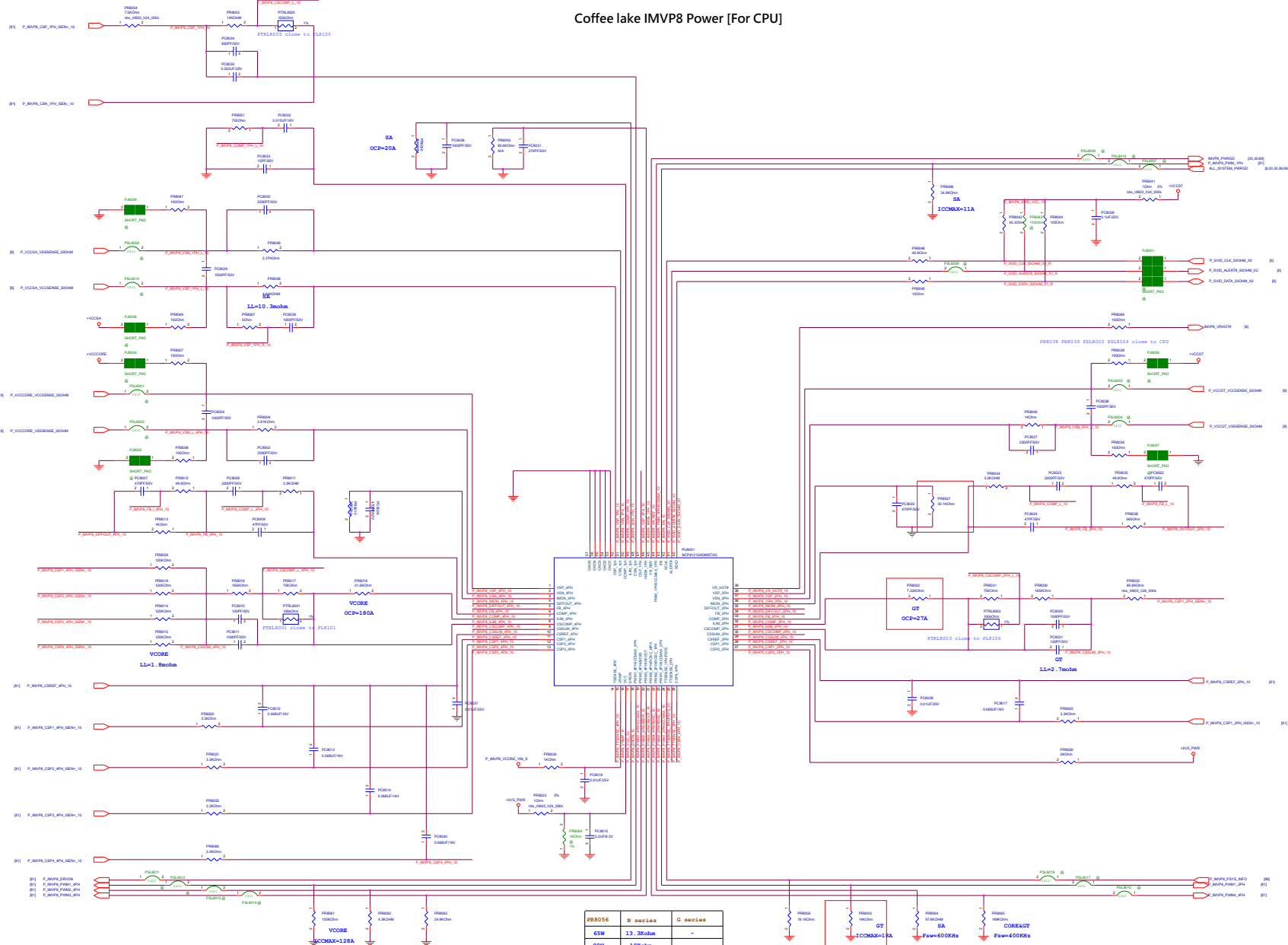
VRAM Thermal Sensor



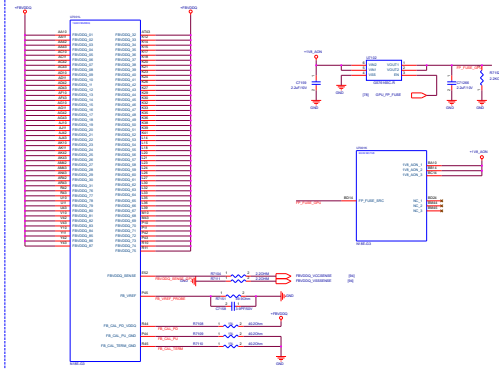
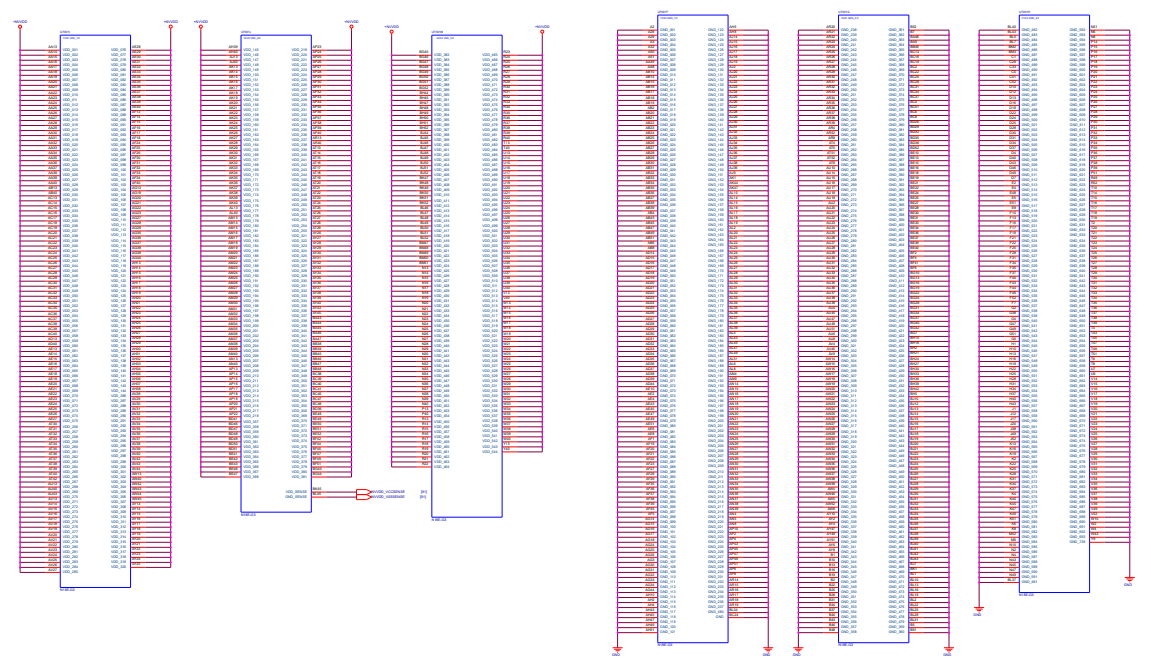




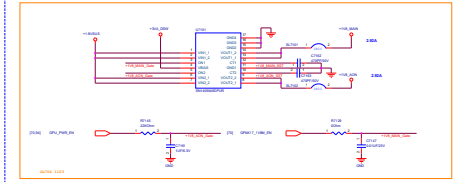
Coffee lake IMVP8 Power [For CPU]



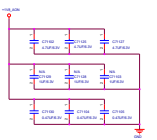
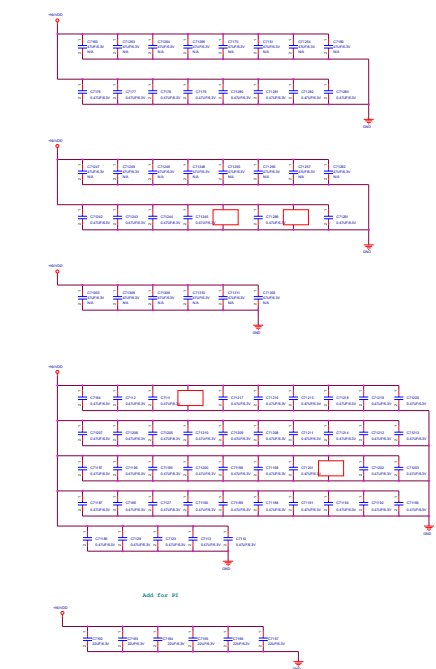
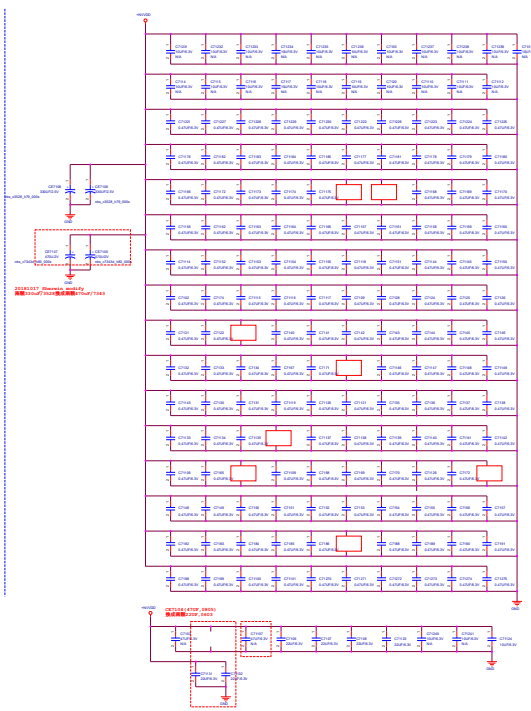
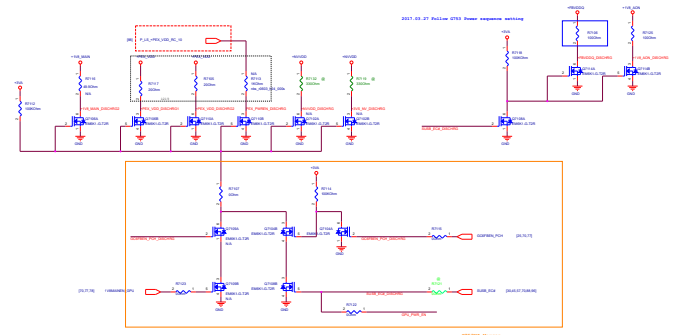
FR8056	N series	G series
65W	13.2Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm



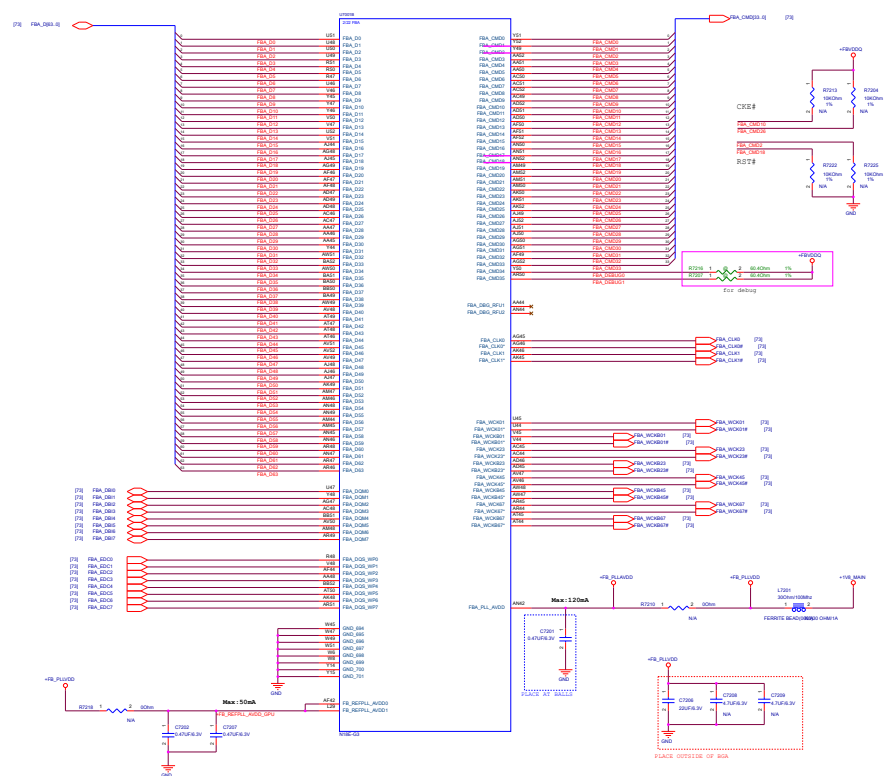
1V8 & 3V3 Power Control



Discharge Discharge

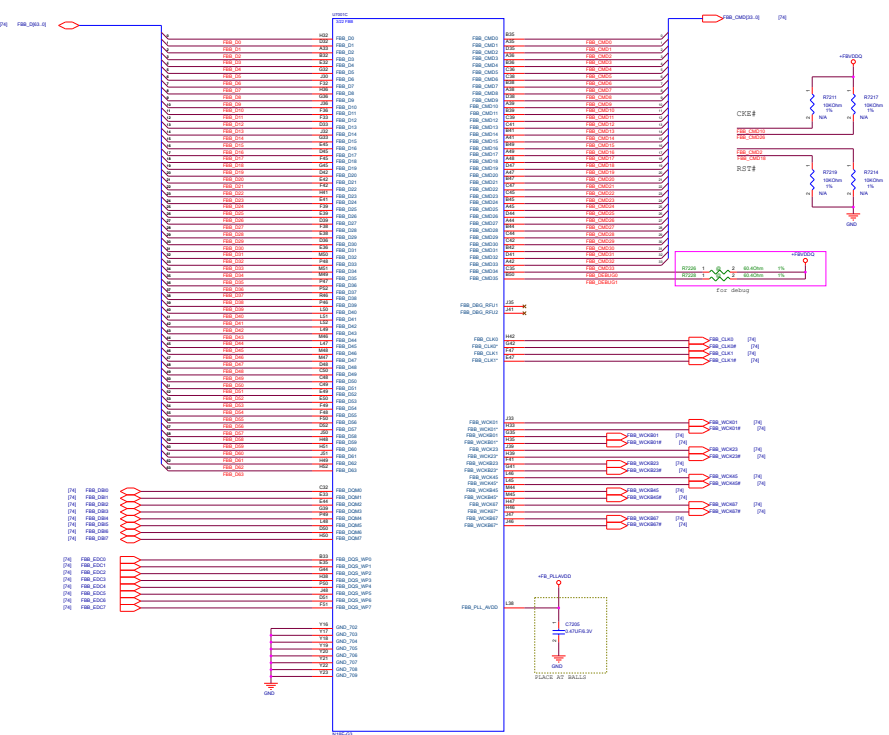


MEMORY: GPU FB Partition A

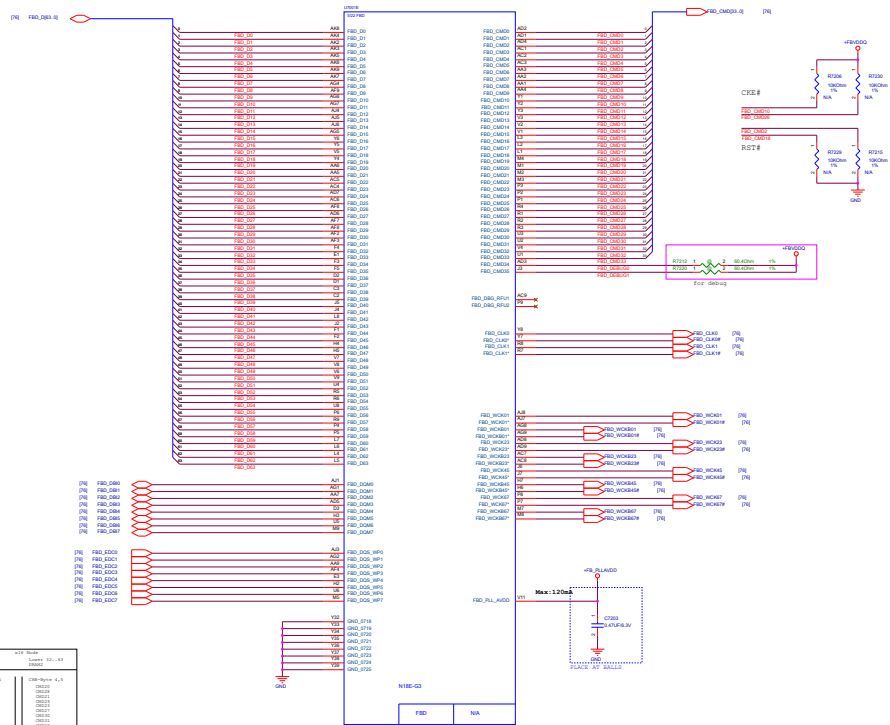


CIS-90: Cystic Fibrosis		Age Range
Gender	Age Range	Age Range
Male	0-10	0-10
Female	0-10	0-10
Male	11-20	11-20
Female	11-20	11-20
Male	21-30	21-30
Female	21-30	21-30
Male	31-40	31-40
Female	31-40	31-40
Male	41-50	41-50
Female	41-50	41-50
Male	51-60	51-60
Female	51-60	51-60
Male	61-70	61-70
Female	61-70	61-70
Male	71-80	71-80
Female	71-80	71-80
Male	81-90	81-90
Female	81-90	81-90
Male	91-100	91-100
Female	91-100	91-100

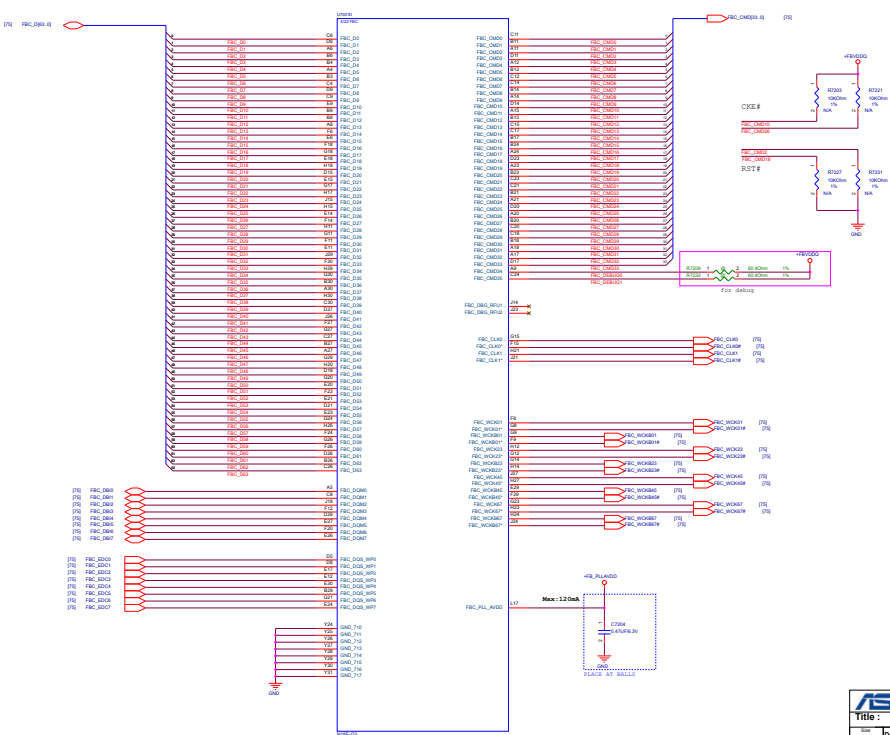
MEMORY: GPU FB Partition B



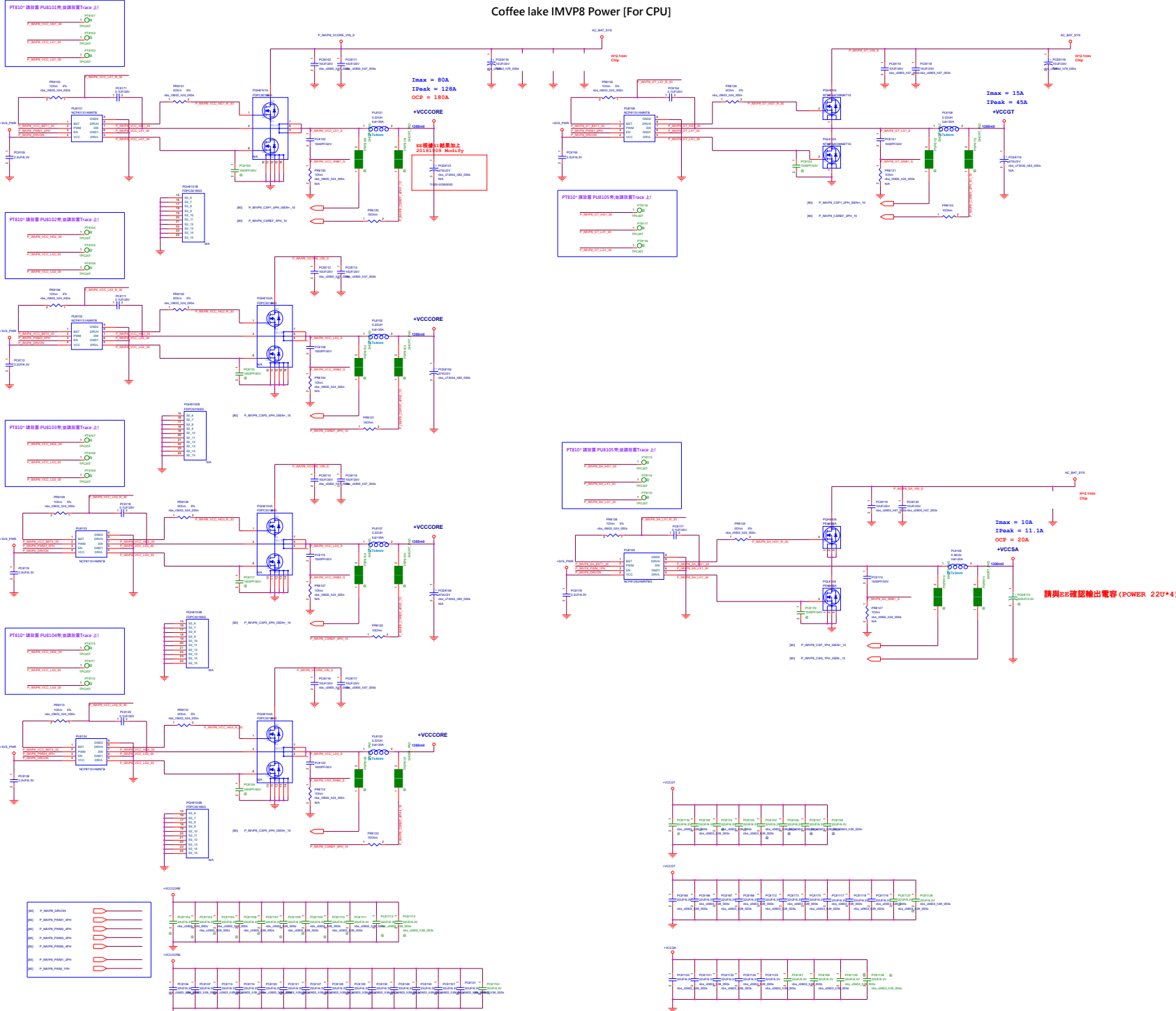
MEMORY: GPU FB Partition D



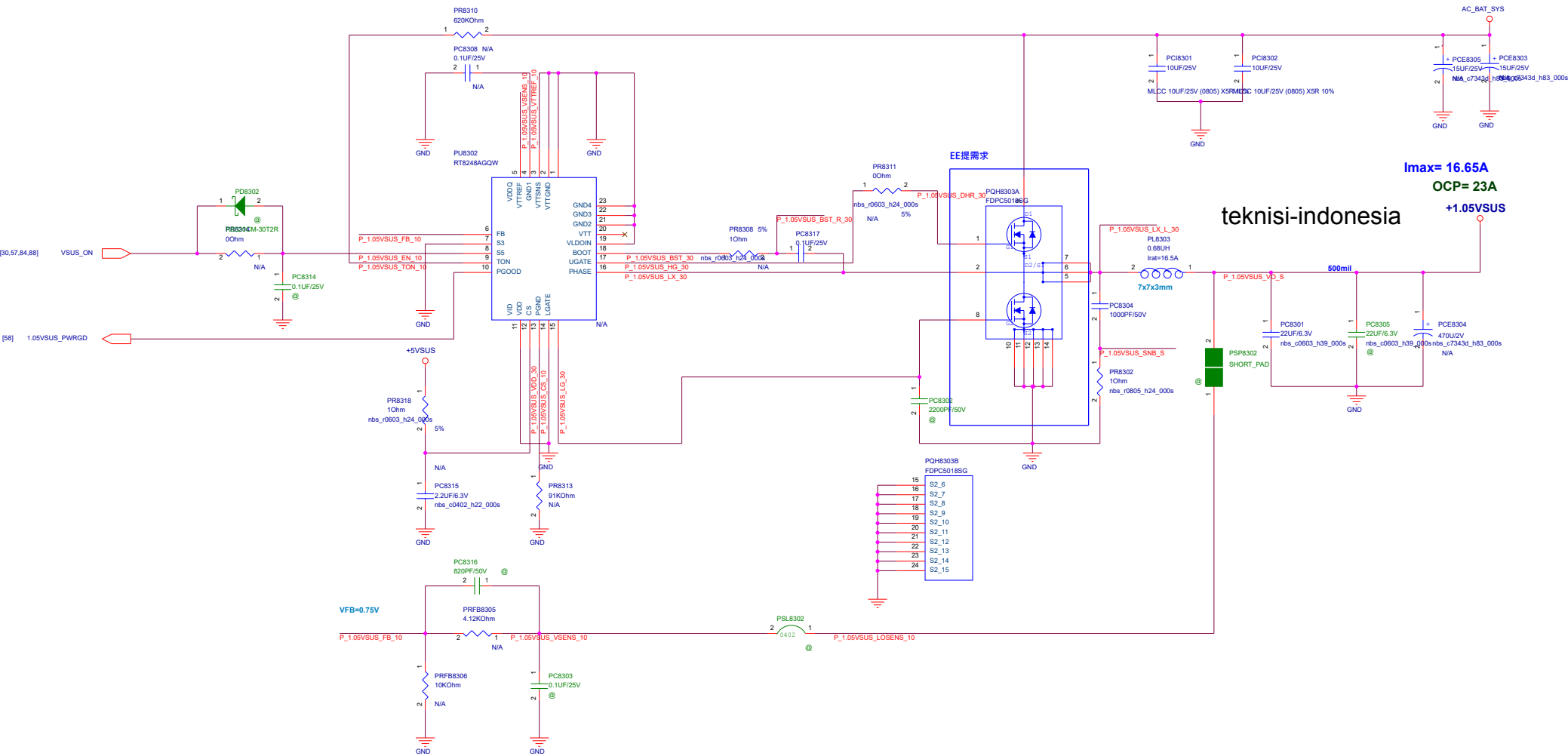
MEMORY: GPU FB Partition C



Coffee lake IMVP8 Power [For CPU]



+1.05VSUS [For PCH]



Imax= 16.65A
OCP= 23A
+1.05VSUS

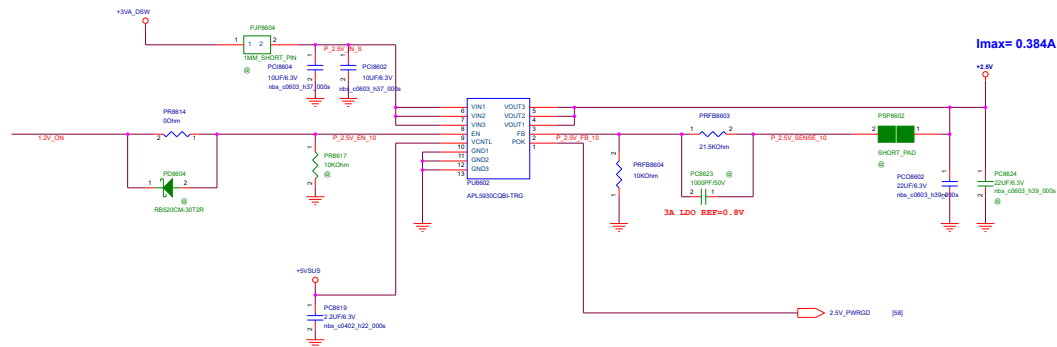
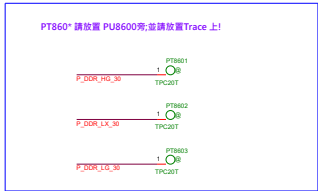
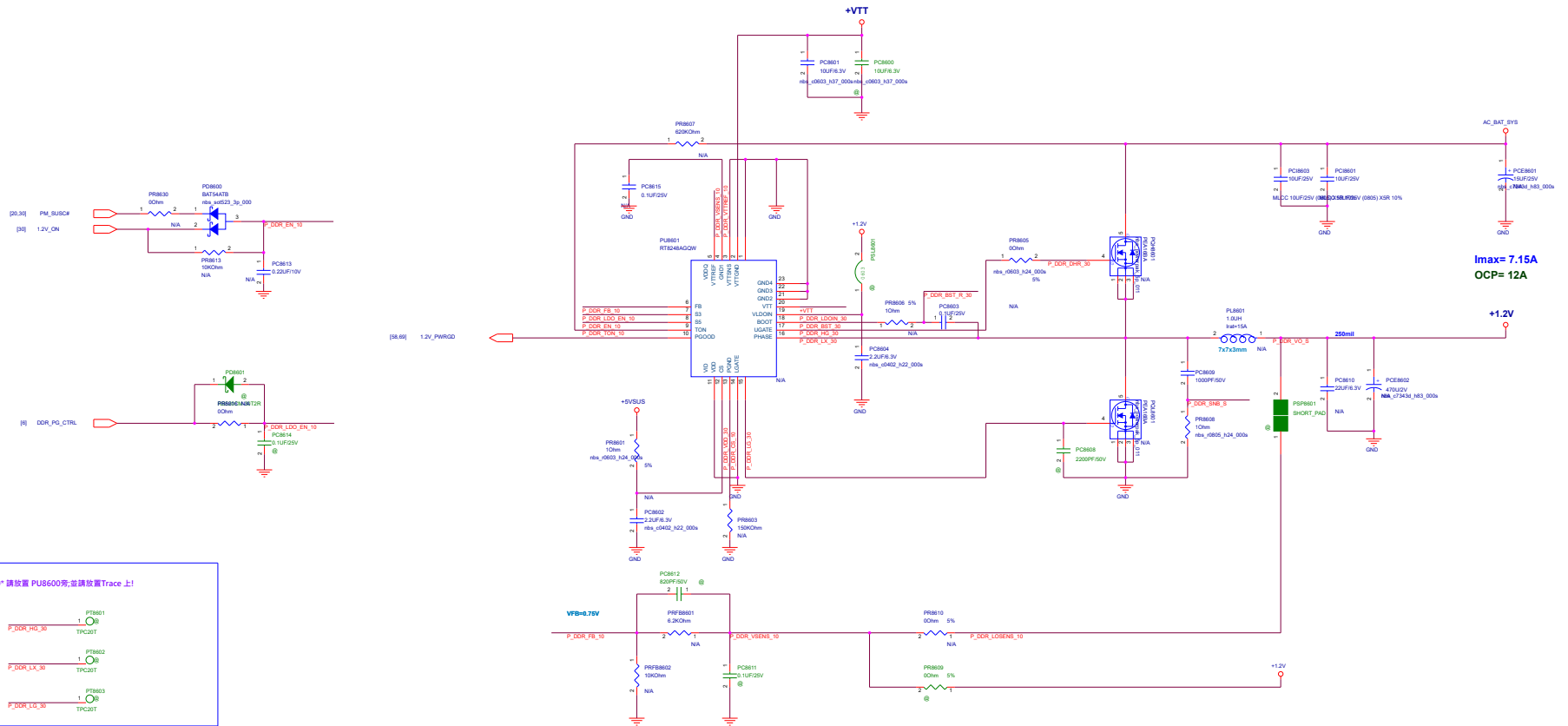
PT830* 請放置 PU8301旁;並請放置Trace 上!

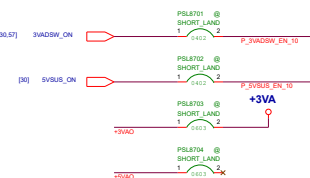
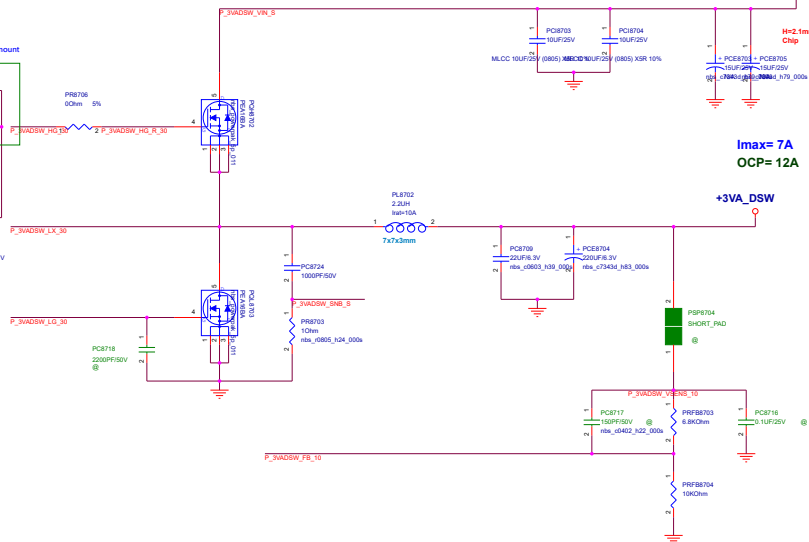
P_1.05VSUS_HG_30

P_1.05VSUS_LX_30

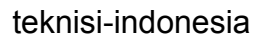
P_1.05VSUS_LG_30

+1.2V / +2.5V [For Memory]

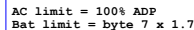




Battery Mode (MVP8)								
	S0	S1	CS	S3	D33	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	-	1	0	0	1
3VADSW_ON	1	-	-	-	1	0	0	0
3VBSW_ON	1	-	-	-	0	0	0	0
5VBSW_ON	1	-	-	-	1	0	0	1
1.35V_ON	1	-	-	-	1	0	0	0
SUSC_ECF	1	-	-	-	0	0	0	0
SUSC_ECF1	1	-	-	-	0	0	0	0

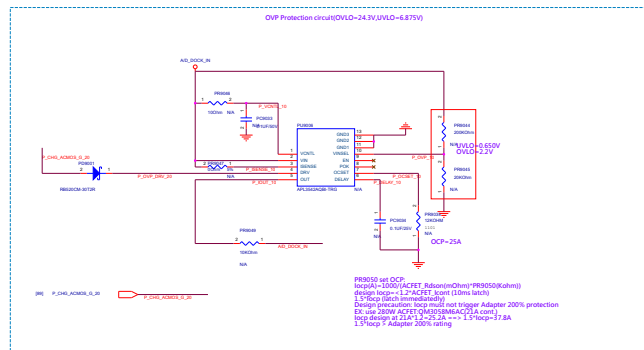
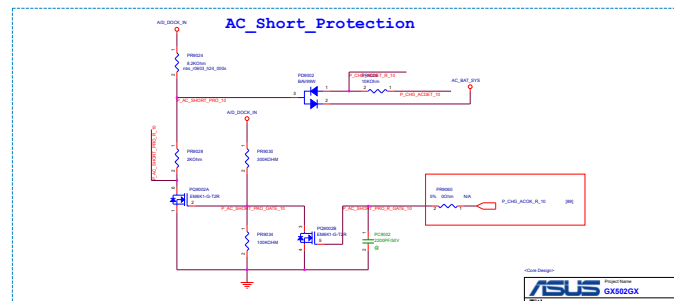
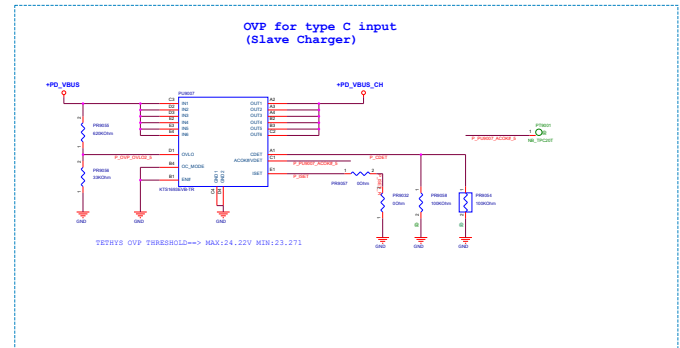
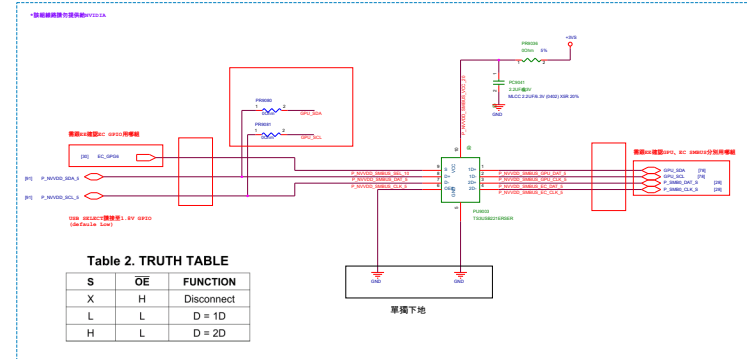
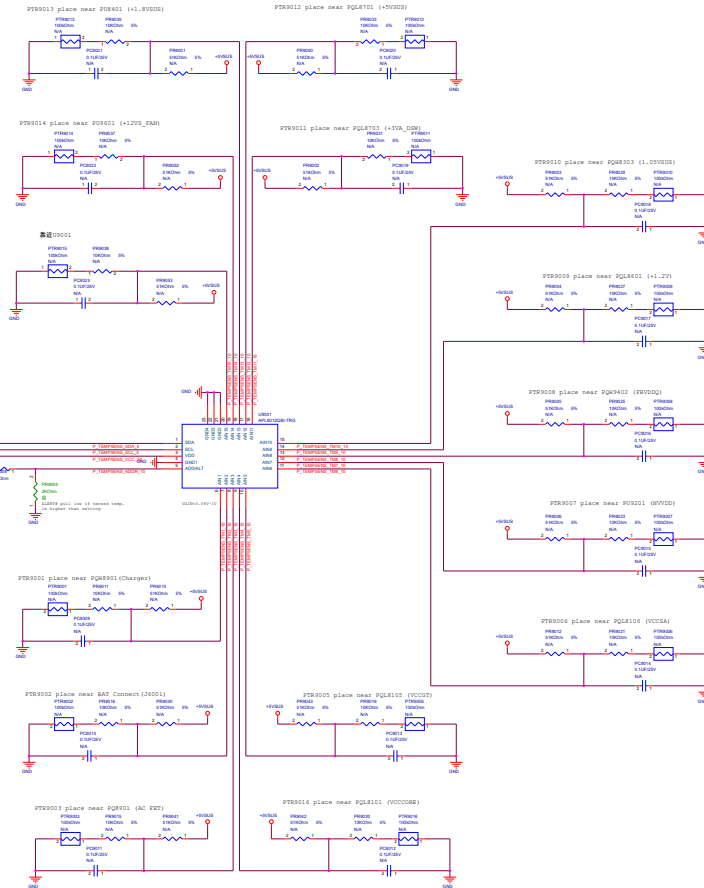


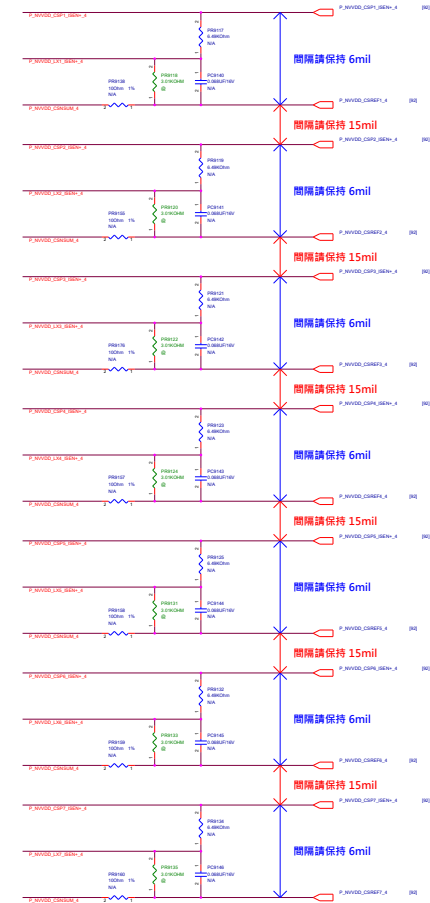
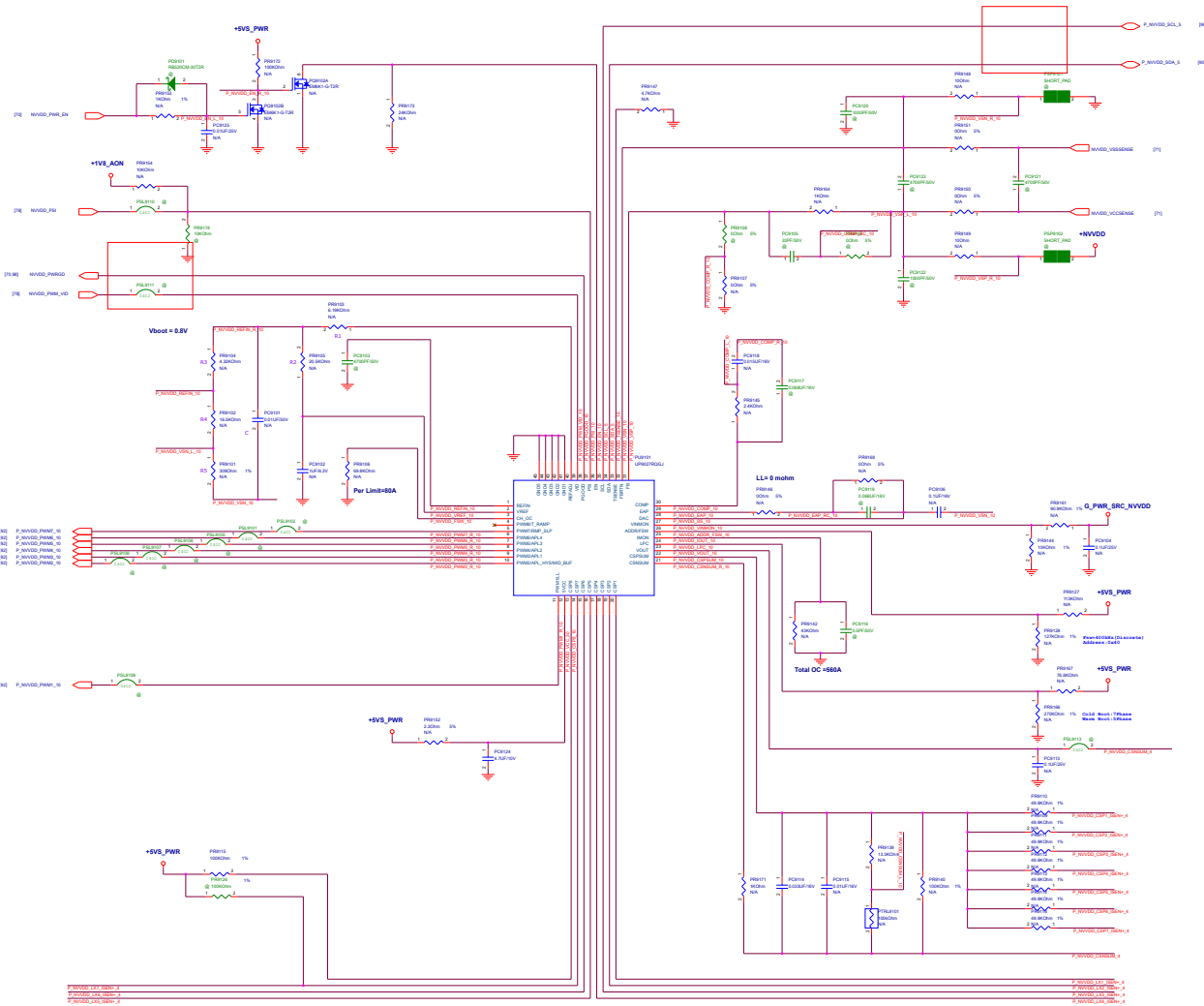
Adaptor select			
		40 Series	50 Series
PR8921		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W



	X X X X	X X X X	X
Function	Temp. alarm threshold setting	Setpoint temp. data	Init 2 = 2 Init 3 = 2 Init 6 = 2 When <u>ALERT</u> occurs

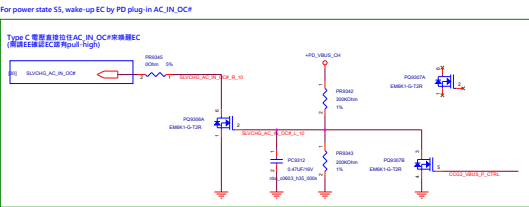
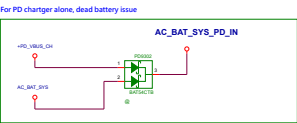
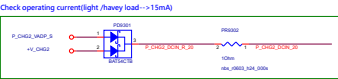
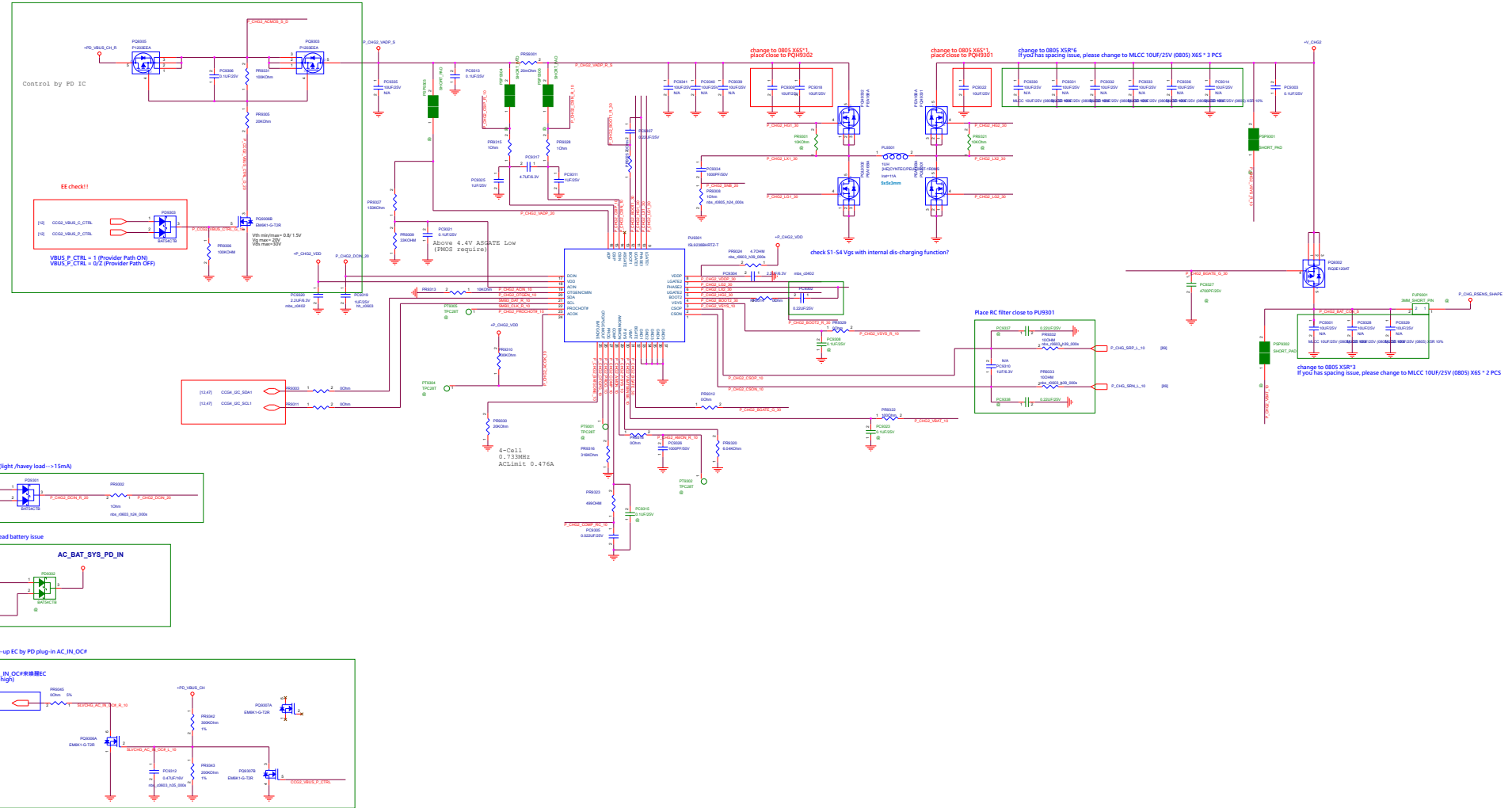
PROTECTION



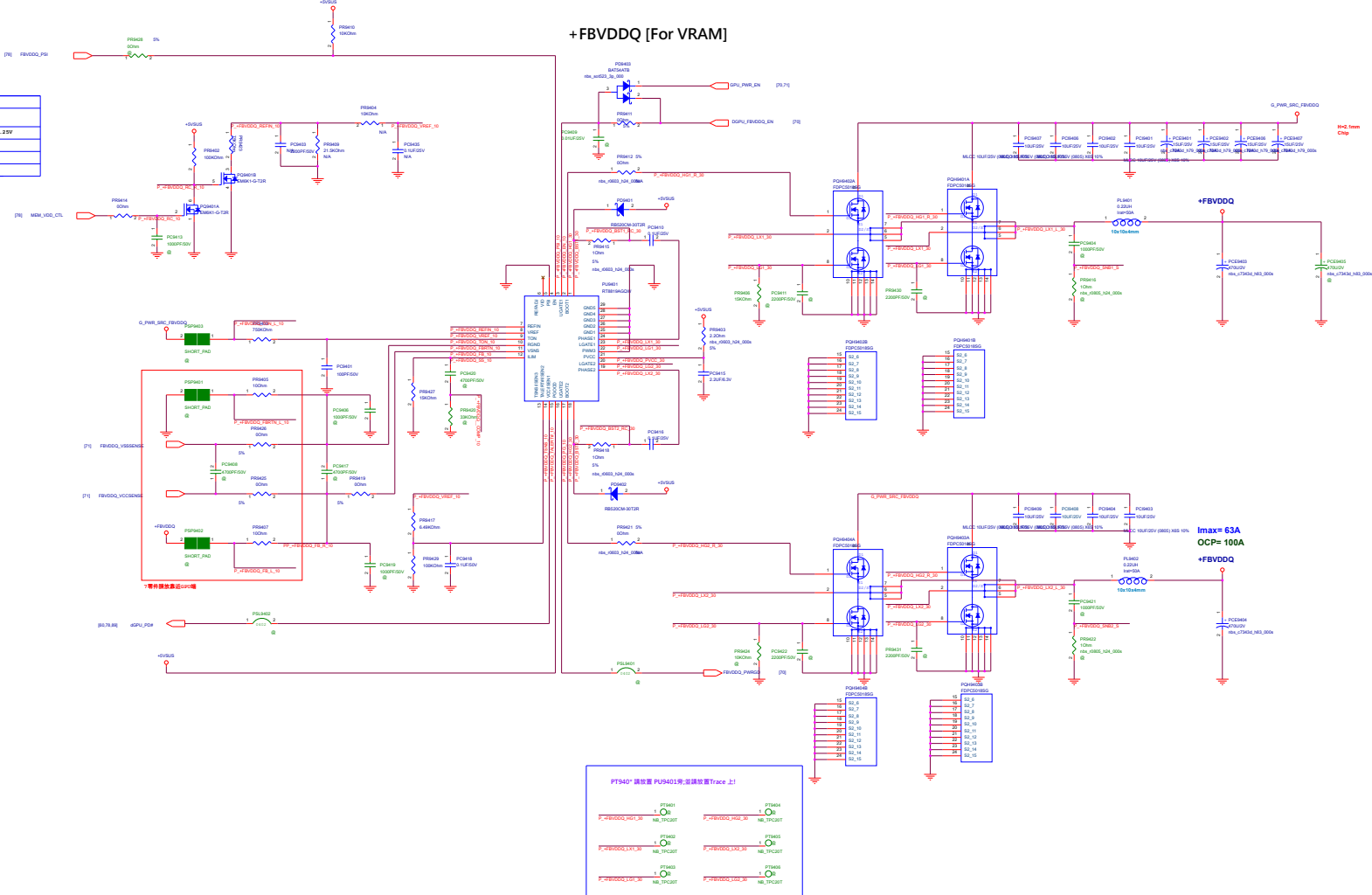


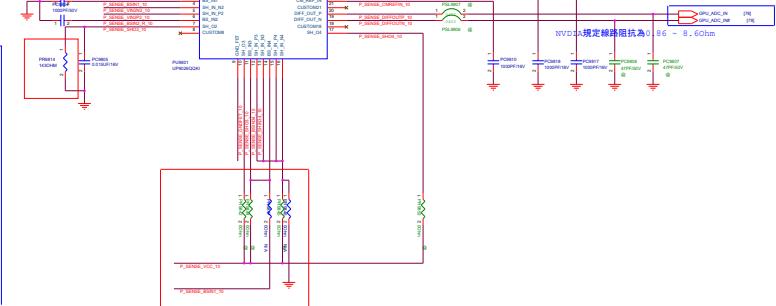
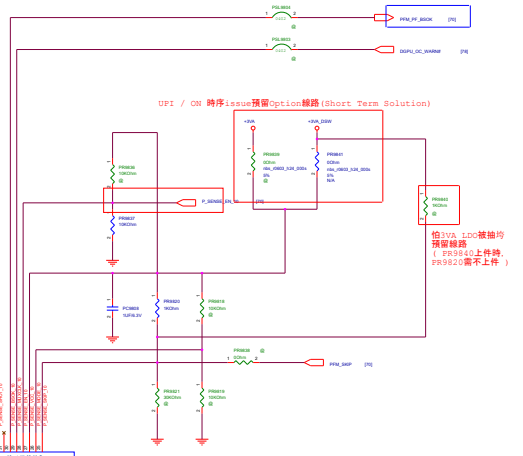
Charger ISL9238B (NVDC)

CYPRESS PD IC VBUS Provider/Consumer control



DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR404	10KOhm	
PR409	21.5KOhm	
PR423	75KOhm	





75W-

[illegible]

75W ~ 90W

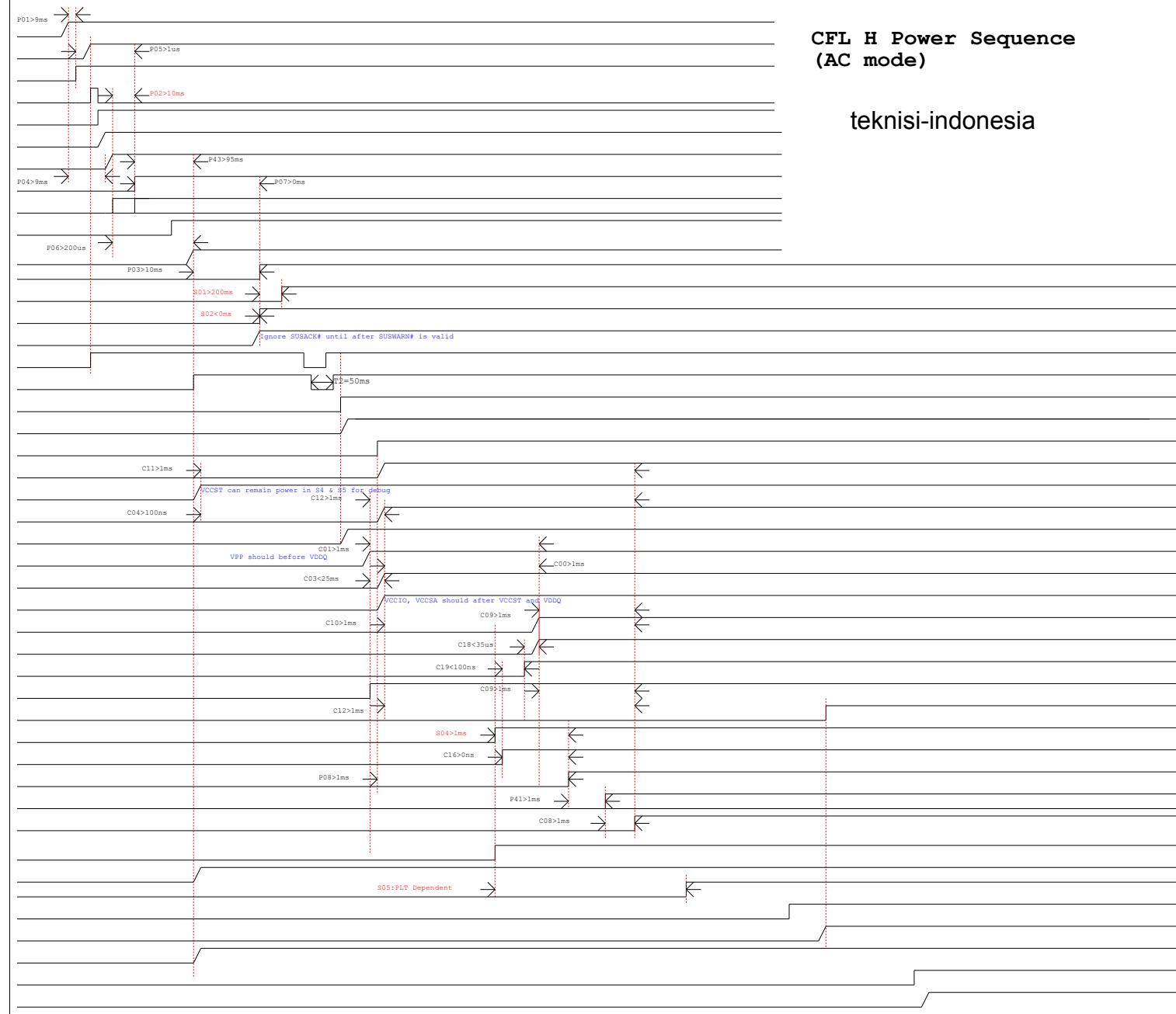
	UP9026PQKI (UPI)	NCP45491 (OM)
FR9801	200a (10G212200014010)	
FR98017	+120 (10102-00571000)	
FR9822	200a (10G212200014010)	
FR9814	+120 (10102-00571000)	
FR9805	03da (10G212330214010)	
FR9806	431a (10102-00581000)	
FR9807	03da (10G212330214010)	
FR9808	431a (10102-00581000)	
FR9811	324ka (10G212324314010)	
FR9812	10da (10G212100214010)	
FR9834	90_9ka (10G212909214010)	

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR_Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(SUSB_EC#)+1.0V_VCCST,VCCPLL
(SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)

(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)

+VCCGT



CFL H Power Sequence (AC mode)

teknisi-indonesia